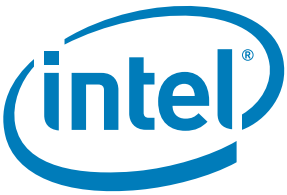

Intel® Core™ 2 Duo Processor and Intel® Core™ Duo Processor with Intel® E7520 Chipset Development Kit

User's Manual

January 2007

Order Number: 316068-001US

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Revision History

Date	Revision	Description
January 2007	001	Initial release.

1.0 About This Manual

This manual describes how to set up and use the evaluation board and other components included in the Intel® Core™ 2 Duo Processor and Intel® Core™ Duo Processor with Intel® E7520 Chipset Development Kit.

1.1 Content Overview

Chapter 1.0, "About This Manual" – Description of conventions used in this manual and instructions for obtaining literature and contacting customer support.

Chapter 2.0, "Getting Started" – Complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3.0, "Theory of Operation" – Information on the system design.

Chapter 4.0, "Platform Management" – Information on the system power management operation.

Chapter 5.0, "Driver and Operating System Support" – List of supported drivers and operating systems.

Chapter 6.0, "Hardware Reference" – Reference information on the hardware, including locations of evaluation board components, connector pinout information, and jumper settings.

Chapter 7.0, "Board Setup Checklist" – Checklist of items to ensure proper functionality of the evaluation board.

Chapter 8.0, "Debug Procedure" – Debug procedure to determine baseline functionality for the Development Kit.

1.2 Text Conventions

The following notations may be used throughout this manual:

 # - The pound symbol (#) appended to a signal name indicates that the signal is active low.

Variables - Variables are shown in italics. Variables must be replaced with correct values.

Instructions - Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.

Numbers - Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character "h". A zero prefix is added to numbers that begin with A through F. For example, FF is shown as 0FFh. Decimal and binary numbers are represented by their customary notations. That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the character "b" is added for clarity.

Signal Names - Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (n). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on;

they are collectively called CSn#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

Units of Measure - The following abbreviations are used to represent units of measure:

A	amps, amperes
GB	GByte, gigabytes
GHz	gigahertz
KB	KByte, kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
MB	MByte, megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

1.3 Technical Support

Support Services for your hardware and software are provided through the secure Intel® Premier Support Web site at https://premier.intel.com. After you log on, you can obtain technical support, review "What's New," and download any items required to maintain the platform. Support is provided through the following product: *Development Kit (Embedded/Core Duo/Core 2 Duo/E7520)*.

1.3.1 Additional Technical Support

If you require additional technical support, please contact your field sales representative or local distributor.

1.4 Product Literature

You can order product literature from the following Intel literature centers.

Table 1. Intel Literature Centers

U.S. and Canada	1-800-548-4725
U.S. (from overseas)	708-296-9333
Europe (U.K.)	44(0)1793-431155
Germany	44(0)1793-421333
France	44(0)1793-421777
Japan (fax only)	81(0)120-47-88-32

1.5 Related Documents

Table 2 is a partial list of the available collateral. For the full lists, contact your local Intel representative.

Table 2. Related Documents

Document	Document Number
Intel® 6300ESB I/O Controller Hub (ICH) Datasheet	Contact your Intel field representative for access.
Intel® E7520 Memory Controller Hub (MCH) Datasheet	
Intel® E7520 Memory Controller Hub (MCH) Specification	
Intel® E7520 Memory Controller Hub (MCH) Specifications Addendum	
Intel® E7520 Memory Controller Hub (MCH) Specifications Embedded Addendum	
Intel® 6700PXH PCI Hub Datasheet	
Intel® 82571EB Gigabit Ethernet Controller Datasheet	
Intel® IMVP-6 Mobile Processor and Mobile Chipset Voltage Regulation Specification	
Intel® Core™ 2 Duo and Intel® Core™ Duo Processor with Intel® E7520 Chipset Platform Design Guide	
Intel® Core™ Duo Processoron 65nm Process Datasheet	
Intel® Core™ 2 Duo Processor for Intel Centrino Mobile technology Datasheet	
Extended Debug Port Design Guide for UP and DP platforms	

2.0 Getting Started

This chapter identifies the Intel® Core™ 2 Duo Processor and Intel® Core™ Duo Processor with Intel® E7520 Chipset Development Kit key components, features and specifications. It also describes how to set up the board for operation. Development software is included in the kit.

Note: This manual assumes you are familiar with basic concepts involved with installing and configuring hardware for a PC or server system.

2.1 Overview

The development kit contains a baseboard with an Intel® Core™ 2 Duo Processor (2.16 GHz), Intel® E7520 MCH, Intel® 6300ESB ICH, and other system board components and peripheral connectors.

Note: The development kit also contains an additional processor, an Intel® Core™ Duo Processor (2 GHz), that can be installed in place of the Intel® Core™ 2 Duo Processor.

Note: The evaluation board is shipped as an open system allowing for maximum flexibility in changing hardware configuration and peripherals in a lab environment. Since the board is not in a protective chassis, the user is required to observe extra precautions when handling and operating the system. Some assembly is required before use.

Note: Review the document provided with the Development Kit titled Important Safety and Regulatory Information. This document contains addition safety warnings and cautions.

2.2 Evaluation Board Features

Table 3 provides an overview of the supported processor pairing for the Intel® E7520 MCH.

Table 3. Supported Processors

Processor Brand	Process	Clock Speed	Front Side Bus	Cache
Intel® Core™ Duo Processor T2500	65 nm	2 GHz	667 MHz	2 MB L2
Intel® Core™ Duo Processor L2400 (BGA Only)		1.66 GHz	667 MHz	2 MB L2
Intel® Core™ 2 Duo Processor T7400		2.16 GHz	667 MHz	4 MB L2
Intel® Core™ 2 Duo Processor L7400		1.5 GHz	667 MHz	4 MB L2

Note: The Intel® Core™ Duo ProcessorL2400 is supported by the Intel® E7520 MCH platform, but a BGA part is not supported by the Customer Reference Board that is included in this Development Kit.

Note: The Intel® Core™ 2 Duo Processor (T7400 and L7400) and the Intel® Core™ Duo Processor (T2500) are supported by the Customer Reference Board that is included in this Development kit. The Customer Reference Board comes with the Intel® Core™ 2 Duo Processor (T7400) installed at the factory. An Intel® Core™ Duo Processor (T2500) is included in the Development Kit and can be installed in place of Intel® Core™ 2 Duo Processor. A separate BIOS flash chip is also included in this kit and must be installed when using the Intel® Core™ Duo Processor.

The evaluation board features are summarized below:

- Intel® Core™ 2 Duo Processor (2.16 GHz) or Intel® Core™ Duo Processor (2 GHz)
  - 667 MHz front side bus
  - On-board processor voltage regulator compatible with IMVP-6 Design Guide
- Intel® E7520 MCH
  - 1 PCI Express* x8 slot
  - 1 PCI Express x4 slot
  - 2 DDR2–400 DIMMs on two channels (4 slots total)
- Intel® 6300ESB ICH
  - From Intel® 6300ESB ICH
    1 PCI 2.2 32/33 Slot
    2 PCI-X 66 MHz slots
    2 IDE connectors
    2 Serial ATA connectors
    2 Serial ports
    4 USB 2.0 ports

  - Super I/O via LPC bus from the Intel® 6300ESB ICH
    1 Floppy port
    1 Parallel port
    1 Serial port
    1 PS/2 port
- Intel® 6700PXH PCI Hub
  - 2 PCI-X 100 MHz slots
  - 1 PCI-X 133 MHz slot
- Intel® 82571EB Gigabit Ethernet Controller
  - 2 Gigabit Ethernet connections
- ITP-XDP debug port
- Port 80 7-segment LEDs
- Board Form Factor - 13” x 16” for benchtop use

2.3 Included Hardware

The following hardware is included in the development kit:

- Intel® Core™ 2 Duo Processor 2.16 GHz, 667 MHz FSB (installed)
- Intel® Core™ Duo Processor 2 GHz, 667 MHz FSB (additional processor)
- Processor heatsink
- Pre-installed jumpers
- Two 512 MB DDR2-400 DIMMs
- Unformatted IDE Hard Drive
- IDE cable
- CD with drivers
- FWH mounted and flashed with the BIOS, additional BIOS chip for the Intel® Core™ Duo Processor
- Standoffs for benchtop use

2.4 Software Key Features

The software in the development kit was chosen to facilitate development of real-time applications based on the components used in the evaluation board. The software tools included are described in this section.

Drivers included:

- Chipset INF Install Utility for Microsoft Windows*
- Optional Intel® 6300ESB ICH driver updates
- Linux* driver packages

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes.

Refer to the documentation in your kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using tools that work with other third party products must have licensed those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third party vendors.

2.4.1 AMIBIOS* for the Development Kit

The evaluation board is pre-installed and licensed with a copy of AMIBIOS* from American Megatrends*.

BIOS updates may be updated periodically. Please contact an field sales representative for BIOS updates.

2.5 Before You Begin

Table 4 presents the additional hardware you may need for your kit.

Table 4. Additional Hardware

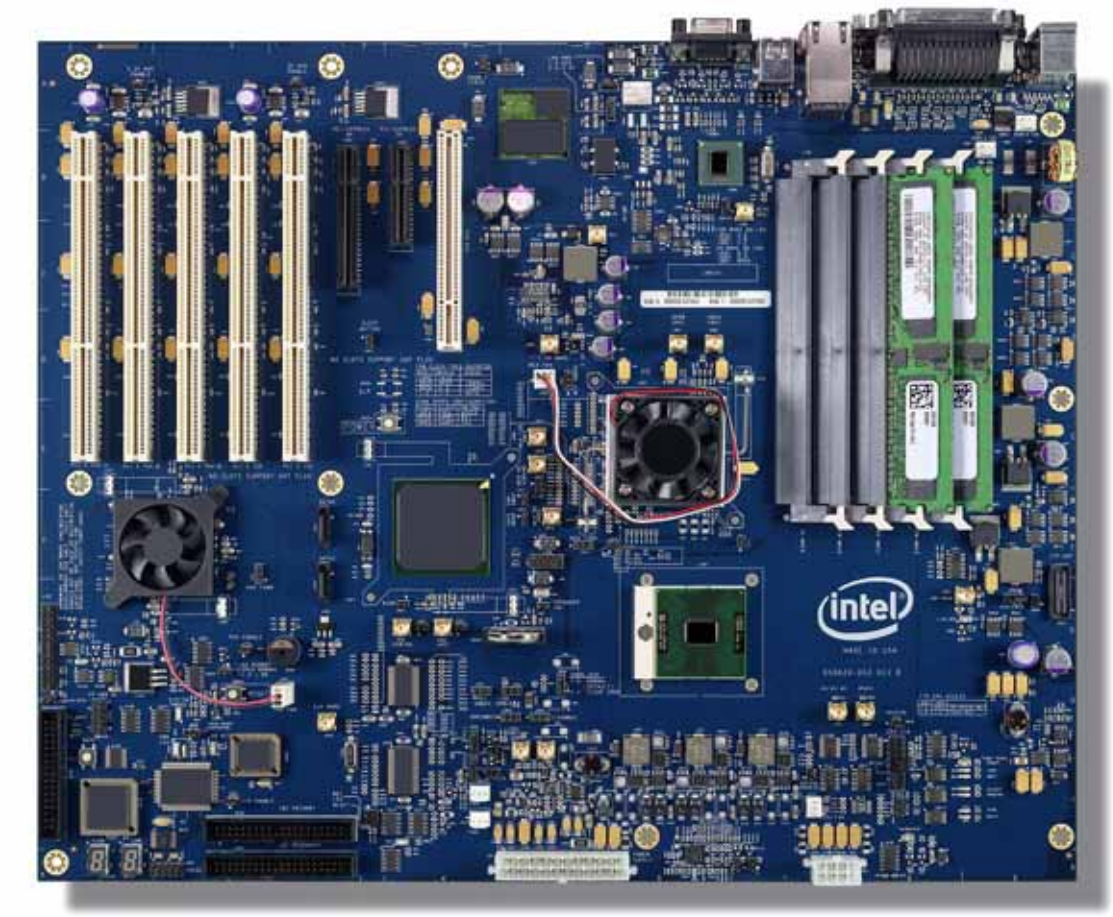
VGA Monitor	You can use any standard VGA or greater resolution monitor.
Keyboard	You can use a keyboard with a PS/2* connector or adapter as well as USB.
Mouse	You can use a mouse with a PS/2* connector or adapter as well as USB.
Hard Drives	You can connect up to four IDE and two SATA devices to the evaluation board.
Floppy Drive (optional)	You can connect a floppy drive to the connector on the evaluation board. No floppy drives or cables are included in the development kit.
Other Devices and Adapters	The evaluation board behaves much like a standard PC motherboard. Many PC-compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card or additional network adapters. You are responsible for procuring and installing any drivers required for additional devices.
450 W or greater SSI 12 V external power supply	Power supply for the Evaluation Board. No power supply is included in the development kit.

2.5.1 Setting up the Evaluation Board

Once you have gathered the hardware described in Section 2.5, follow the steps below to set up the development kit. This manual assumes you are familiar with basic concepts involved with installing and configuring hardware for a PC or server system.

Note: Review the document provided with the Development Kit titled Important Safety and Regulatory Information. This document contains addition safety warnings and cautions.

Figure 1. Evaluation Board Before Installing Additional Hardware



2.5.2 Safety

Ensure a safe work environment. Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge, which may cause product failure or unpredictable operation.

Caution: Connecting the wrong cable or reversing a cable may damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

Warning: Make sure AC cord of power supply is unplugged before performing the following steps in Section 2.6.

2.5.3 Package Contents

Verify kit contents. Inspect the contents of your kit and ensure that everything listed in Section 2.3 is included. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Check jumper settings. Verify that the jumpers are set in their default state. Refer to Section 6.4 for detailed descriptions of all jumpers and their default settings indicated in bold.

2.5.4 Installed Hardware

Verify installed hardware. Make sure the following hardware is populated on your evaluation board:

- Intel® E7520 MCH heatsink
- Intel® 6700PXH PCI Hub heatsink
- BIOS FWH
- Battery in holder

Caution: The above hardware should have been correctly installed at the factory. If components are not installed correctly, DO NOT power on the board. Correctly re-install the components before proceeding. If you suspect that any of the kit components have been damaged, contact your Intel field sales representative or local distributor for assistance.

2.5.5 Installing Standoffs

The evaluation board in this development kit is shipped as an open system allowing for maximum flexibility in changing hardware configuration and peripherals in the lab environment. Since the board is not in a protective chassis, the user is required to observe extra precautions when handling and operating the system.

The board is a standard ATX form factor and provides non-plated mounting holes with top and bottom ground rings. If the board is not going to be used in a chassis, standoffs are included for bench top use in the lab environment.

The development kit includes eight standoffs and eight screws that you can use to attach to the board for bench top use. Standoffs should be attached to board at the following mounting hole locations, A1, A4, A9, E1, E3, K1, J6, and J9.

1. Insert screw through top mounting hole.
2. Place standoff on back side of board and hand tighten to screw.
3. Repeat for additional standoffs on the board until all eight standoffs are installed.

2.5.6 Installing the Heatsinks for Processor and MCH

Heatsink Installation: In order for the board to operate properly, a heatsink must be installed on the processor and on the Intel® E7520 MCH. **DO NOT** power on board without a processor thermal solution. Heatsinks may already come pre-installed on the MCH. Please refer to this section if you need to remove or re-install the heatsinks.

Tools Needed: Flat head screwdriver and Phillips head screwdriver

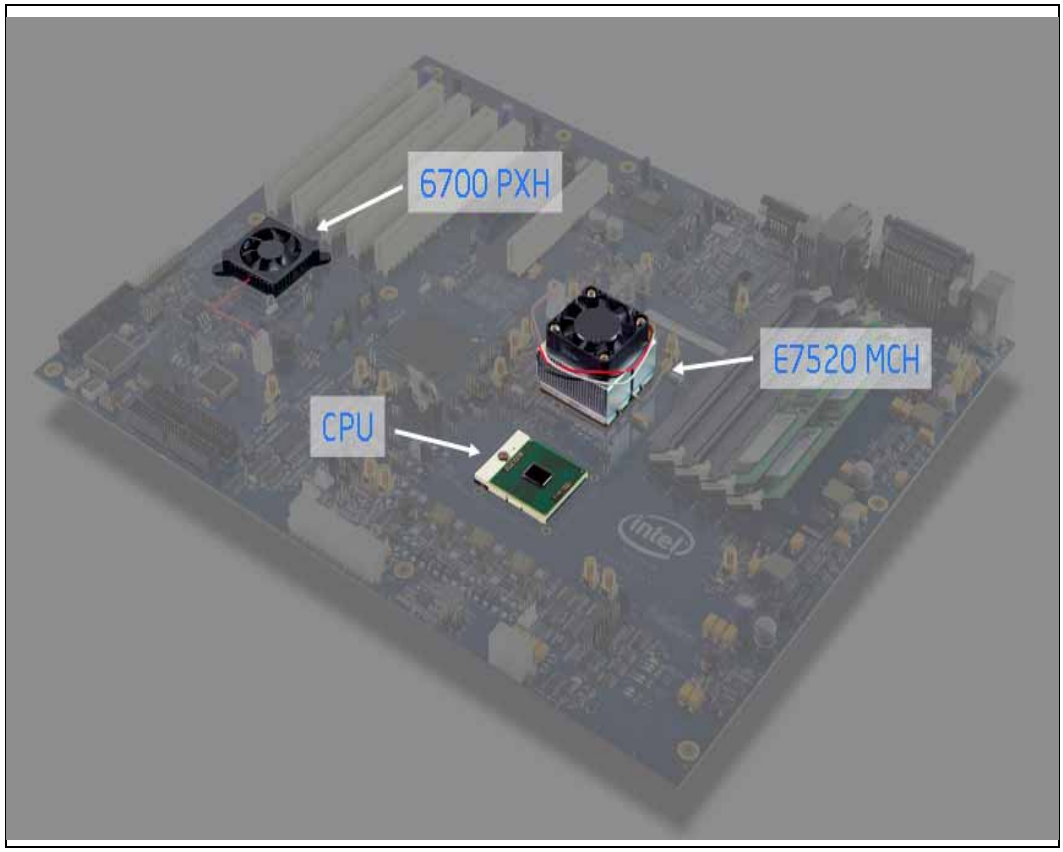
Consumable Items Needed: Disposable towels and isopropyl alcohol

Note: Processor heatsink may be silver or copper in color.

Table 5. Heatsink Information

Component	Quantity Per Board	Heatsink Manufacturer	Part Number	Comments
Processor	1	Cooler Master*	EEP-N41CS-01-GP	Active heatsink and back plate
Intel® E7520 MCH	1	Cooler Master*	ECB-00208-03-GP	Active heatsink
Intel® 6700PXH PCI Hub	1	Sunon*	GC123506BH-8DA.05.N.B515GN/ 2026GN	Active heatsink

Figure 2. Location for the Processor, MCH, and PXH for Heatsink Installation



Caution: Applying excess pressure may cause damage to the processor.

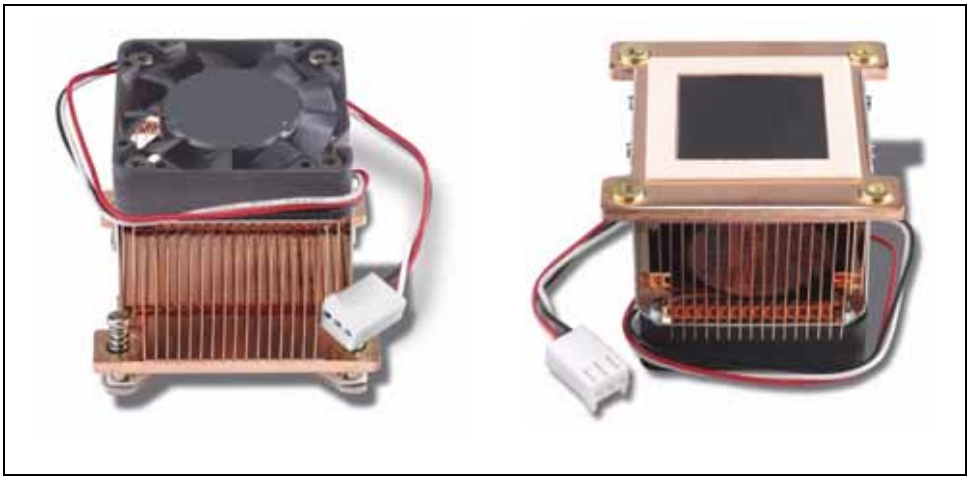
Note: Do not turn power on until the processor thermal solution has been installed.

2.5.7 Processor Heatsink Installation

This section details how to install the processor heatsink.

Note: If the Thermal Interface Material (TIM) is scratched, scrape it off and replace with new material. If a replacement is needed, use a TIM with high thermal conductivity such as thermal grease or a phase change material. The gasket ensures the heatsink is sitting flat on the package.

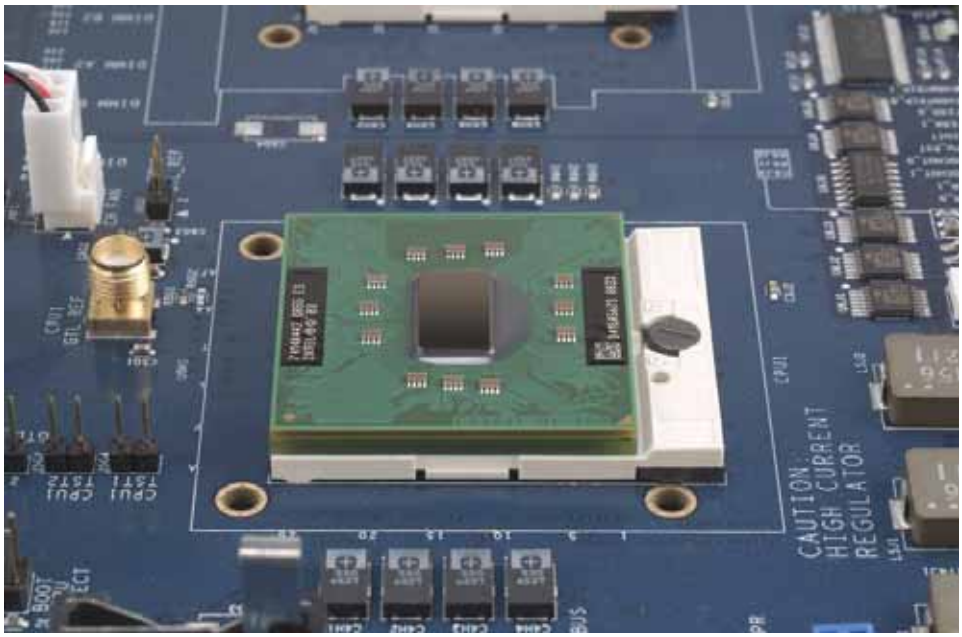
Figure 3. Processor Heatsink Top and Bottom View



1. Make certain that the processor is firmly seated in socket U6G1, and the package is secured using a flathead screwdriver.

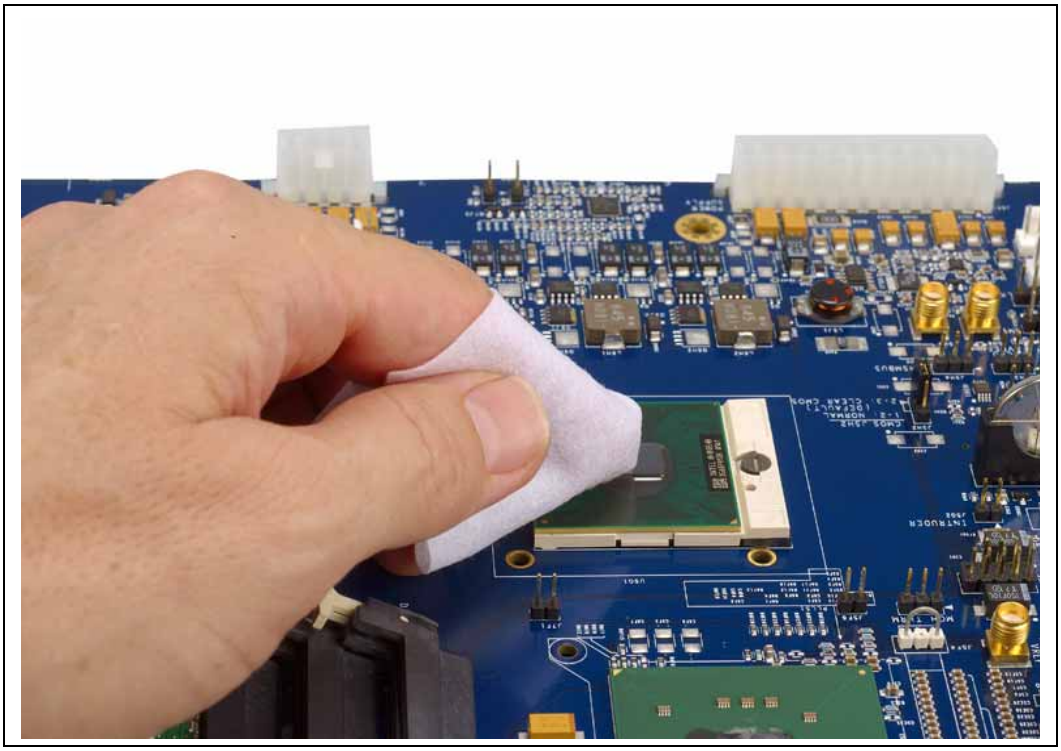
Note: The processor socket has a screw locking mechanism. The socket has an indication to show if the processor is locked in place. To remove the processor, turn the screw counter-clockwise all the way until it stops. The processor will be loose and will come out easily. To insert the processor, line up the socket and processor corners that do not have pins and insert the processor in the socket. Turn the screw clock-wise until it is tight and the processor is firmly held.

Figure 4. Processor in Socket and Package Secured



2. Clean the top surface of the processor die with a clean towel and isopropyl alcohol (IPA).

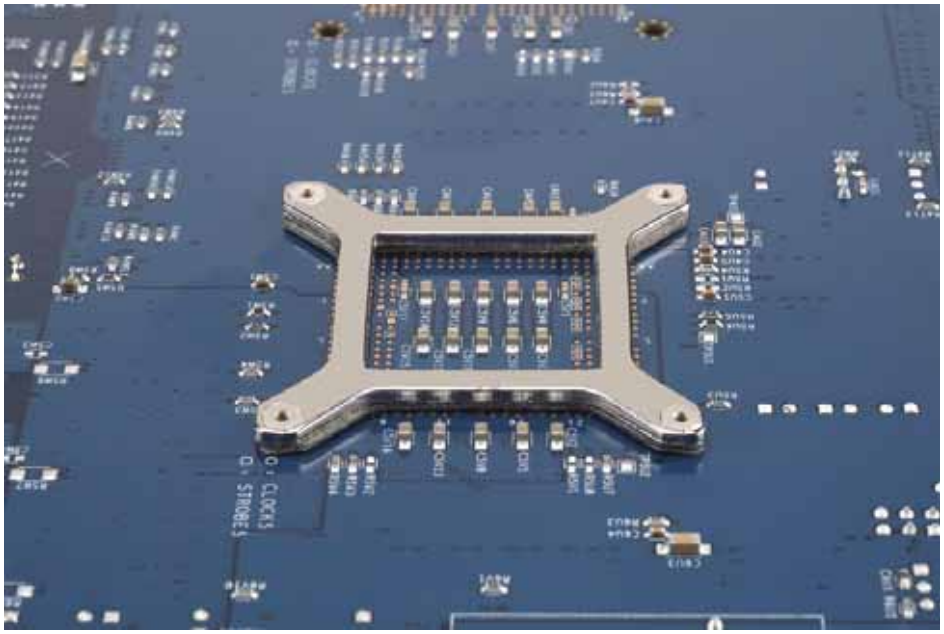
Figure 5. Clean Top of Processor Die



3. Install the back plate to the bottom side of the PCB at the processor location. Align the standoffs to the four mounting holes in the board.

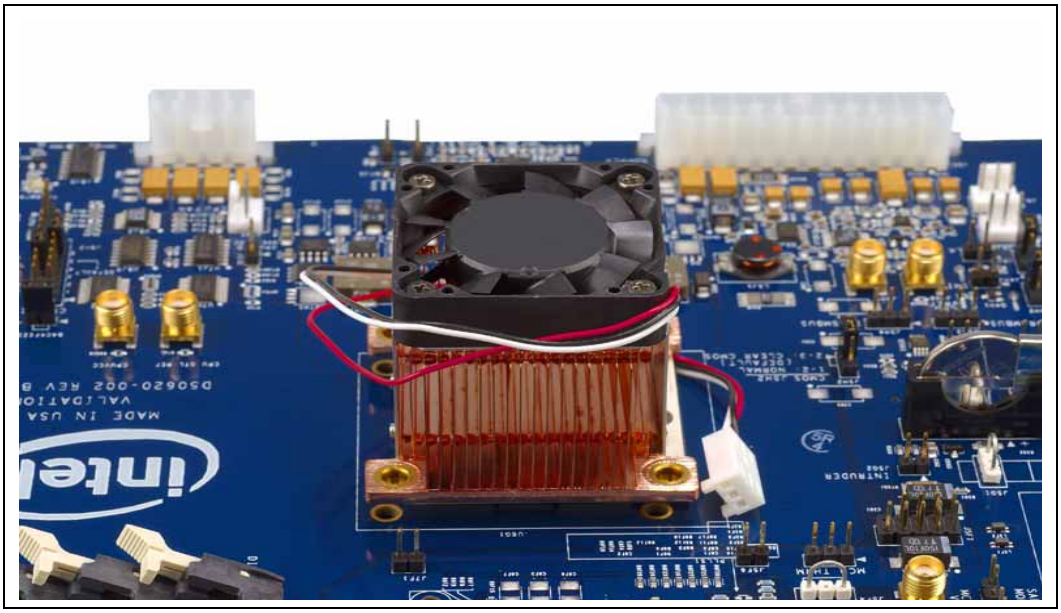
Note: There is a non-electrically conductive tape to hold the back plate in place until the heatsink is completely installed.

Figure 6. Back Plate in Place



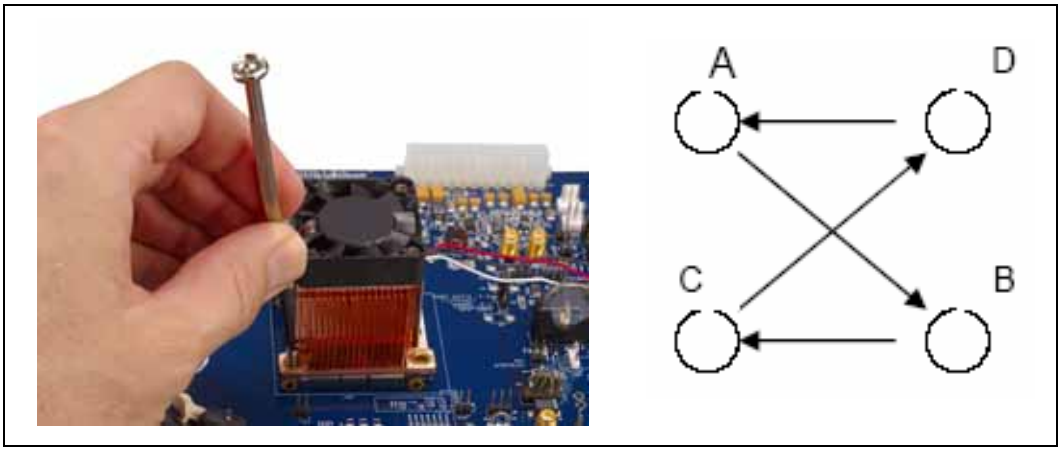
4. Mount the heatsink to the processor. Ensure the TIM and die have contact.

Figure 7. Heatsink Mounted on Processor



5. Align the screws (4x at corners) to the threaded holes of the standoffs on the back plate. Using the Phillips head screwdriver, tighten the four screws in a diagonal manner (as shown in the diagram). Tighten each screw half of the screw length for A to B and follow by ¼ for C to D. Then tighten A to B until the screw hard stops and repeat for C to D. The screws are designed to compress the springs a predetermined amount.

Figure 8. Screw Tightening Order



6. Plug the fan connector to the fan pin header J7J1 on the board.

Note: The heatsink removal process is the reverse of the installation procedure.

2.5.8 MCH Heatsink Installation

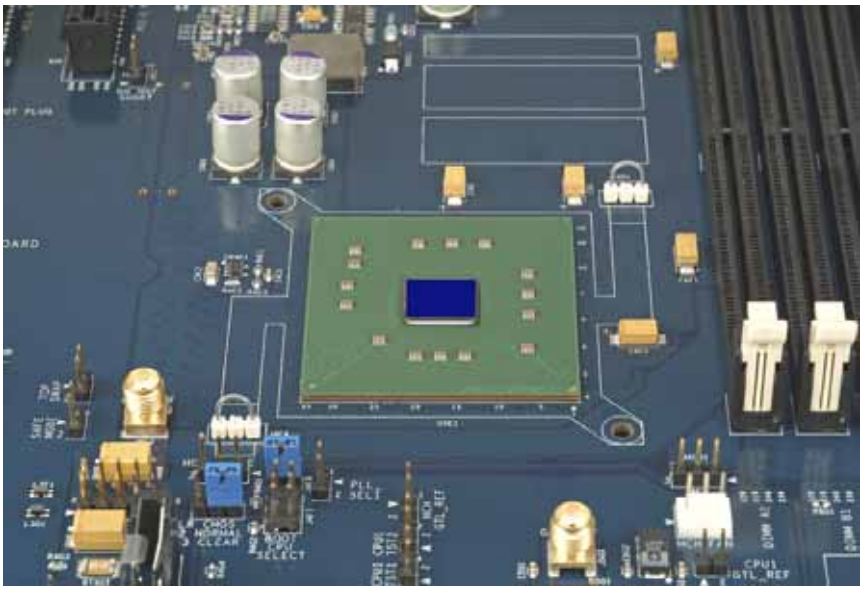
This section may not apply if the MCH heatsink is pre-installed on the board. However, you may want to briefly look over the procedure to verify that the heatsink is properly installed and it has not been damaged in the packaging.

Note: If the Thermal Interface Material (TIM) is scratched, scrape it off and replace with new material. Use a TIM with high thermal conductivity, such as thermal grease or phase change material.

Figure 9. MCH Heatsink Top View

1. Clean the top surface of the MCH die with a clean towel and isopropyl alcohol (IPA).

Figure 10. Clean Top of MCH Die

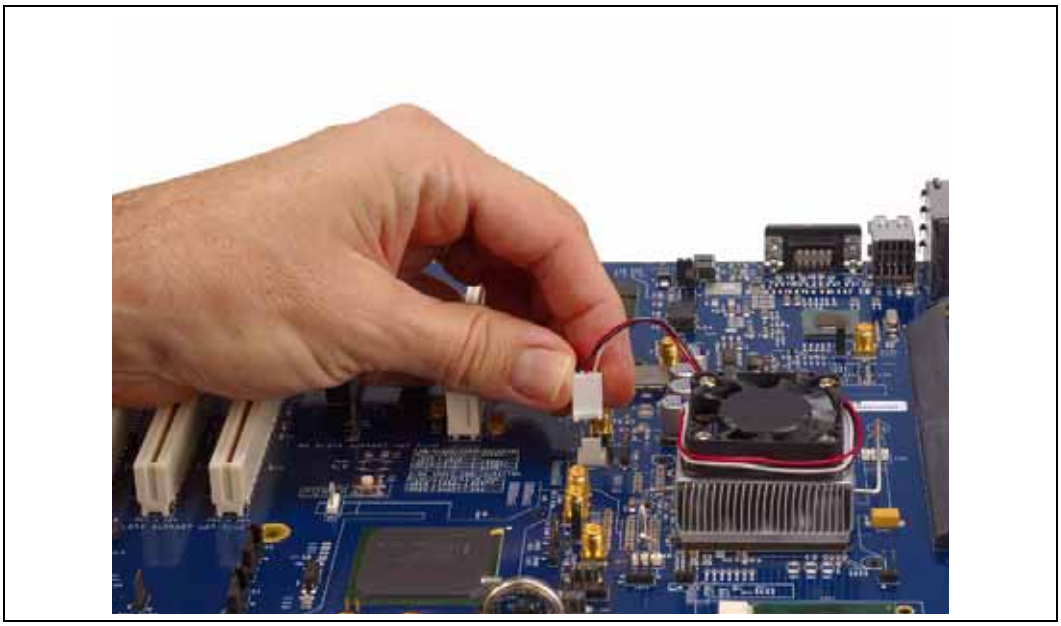


2. Hook one end of the heatsink clip to one of the anchors located near the corner of the MCH. Securely hold the other end of the heatsink clip.

Figure 11. Hook Heatsink Clip to Anchor

3. Hold the clip firmly to the anchor to prevent the heatsink from moving. Attach the other end of the clip to the other anchor. Ensure that the heatsink is level with the MCH package.

Figure 12. Heatsink Fan Connector



4. Plug the fan connector to the fan pin header J5D2 on the board.

Note: The heatsink removal process is the reverse of the installation procedure.

2.5.9 Installing Memory

The kit includes two 512 MByte registered ECC DIMMs. To install, ensure the tabs on the slot are open, or rotated outward from the slot. Line up the DIMM above the slot (the DIMM is keyed so that it only fits in the slot in one orientation). Firmly but carefully insert the DIMM into the slot until the tabs close. Repeat for all other DIMM and slots.

Note: When populating both channels, always place identical DIMMs in sockets that have the same position on channel A and channel B (i.e., DIMM A2 should be identical to DIMM B2).

Note: Populate DIMMs starting with the sockets farthest away from the MCH (DIMM slots A2 and B2).

Caution: Do NOT bend the board when installing memory. There are a large number of components near the memory slots and excessive board flex can lead to solder joint failure.

2.5.10 Installing Storage Devices

There is two IDE connectors on the evaluation board, which supports an IDE devices. For a correct boot-up of the system, ensure that a hard drive is installed as the primary master. (Master/slave settings are determined by a jumper on each IDE device. Consult the device label/documentation to verify that the jumper is set correctly for any configuration you choose.) A CD-ROM drive or additional hard drive may be installed as a primary slave device. Follow this procedure to install a hard drive on the evaluation board:

1. Verify that the jumper on the hard drive is set correctly for single or master, depending on your configuration.
2. Install the hard drive. This can be done using either the IDE or SATA.

IDE Installation:

a. Connect the long end of the IDE cable to the IDE connector J2J2 on the board. Ensure that the red line (pin one on the cable) is aligned with pin one of the connector indicated by an arrow.

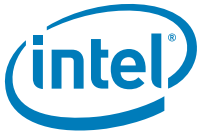
b. Connect the middle connector of the cable to the hard drive. Again, ensure that the red line, pin one on the cable, is aligned with pin one on the hard drive.

Note: Failure to properly align the IDE cable may damage the evaluation board and/or the hard drive.

SATA Installation:

a. Connect one end of the SATA cable to the hard drive connection. Connect the other end to the SATA0 or SATA1 connector (J3F1 or J3F2, respectively) on the board.

3. Connect a power connector from the power supply to the hard drive. The power connector on the SATA drive may have a plastic cover that will need to be removed. (Old style power connector is supported.)
4. Install the CD-ROM drive (optional). A CD-ROM drive is not included in the kit and is not required, but you may find it useful in loading additional software. To install it on the evaluation board:
   a. Verify that the jumper on the CD-ROM drive is set for slave.
   b. Connect the unused end of the IDE cable to the CD-ROM drive. Ensure that the red line, pin one on the cable, is aligned with pin one of the CD-ROM drive connector, indicated by an arrow.
   c. Connect a large 4-pin power connector from the power supply to the CD-ROM drive.
5. Install the floppy drive (optional). A floppy disk drive is not included in your kit and is not required, but you may find it useful in loading additional software. To install a floppy drive on the evaluation board:
   a. Connect the floppy cable to the floppy connector J1J1. Ensure that the red line (pin one on the cable) is aligned with pin one of the connector, indicated by an arrow.
   b. Connect the other end of the floppy cable to the floppy drive.
   c. Connect a power cable to the floppy drive. Ensure that the red line (pin one on the cable) is aligned with pin one on the floppy drive.



2.5.11 Connect the Monitor Cable

Connect the monitor cable to J6A1 on the evaluation board. If using a video card disable onboard video by removing jumper J4A1, insert video card and connect monitor cable to video connector on card.

Note: Monitor is not included in this development kit.

2.5.12 Connect the Keyboard and Mouse

Connect a PS/2* mouse and keyboard to the stacked PS/2* connector on the evaluation board. The bottom connector, often purple, is the keyboard connector and the top, often green, is the mouse connector. Alternatively, you may plug a USB keyboard and a USB mouse into the USB connectors on the evaluation board.

Note: Keyboard and mouse are not included in this development kit.

2.5.13 Connect the Power Supply

Make sure the power supply is turned off and unplugged. Connect the two ATX power supply cables to connectors J5K1 and J8K1 on the evaluation board. Next, plug the power cord into the power supply and the wall. Then turn on the switch on the back of the power supply.

Note: Power Supply is not included in this development kit. Use power supply described in Section 2.5.

2.5.14 Power the System

Turn on the monitor and then turn on the evaluation board.

Note: Do not turn power on until the processor thermal solutions have been installed.

Caution: Ensure that fan heatsink on the processor is operational. If not, turn off the power immediately and verify that the fan heatsink is connected to the board correctly (see Section 2.5.6). If the fan heatsink is not operating, contact your Intel field sales representative or local distributor.

2.6 Configuring the BIOS

An AMI* BIOS is pre-loaded on the evaluation board. You may need to make changes to the BIOS to enable hard disks, floppy disks and other supported features. You may use the setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface.

On first boot-up of the system, you may want to use the BIOS setup program to verify the date/time and boot device. BIOS updates may periodically be posted to the Intel Developer web site at http://developer.intel.com/design/intarch. Pressing the Delete key during boot causes the system to enter into the BIOS setup program.

The development kit contains an additional BIOS chip for use with the Intel® Core™ Duo Processor. To replace the BIOS chip, follow the following steps:

- Remove power from the CRB
- Remove FWH from U2H3
- Install new FWH in U2H3
- Apply power to the CRB

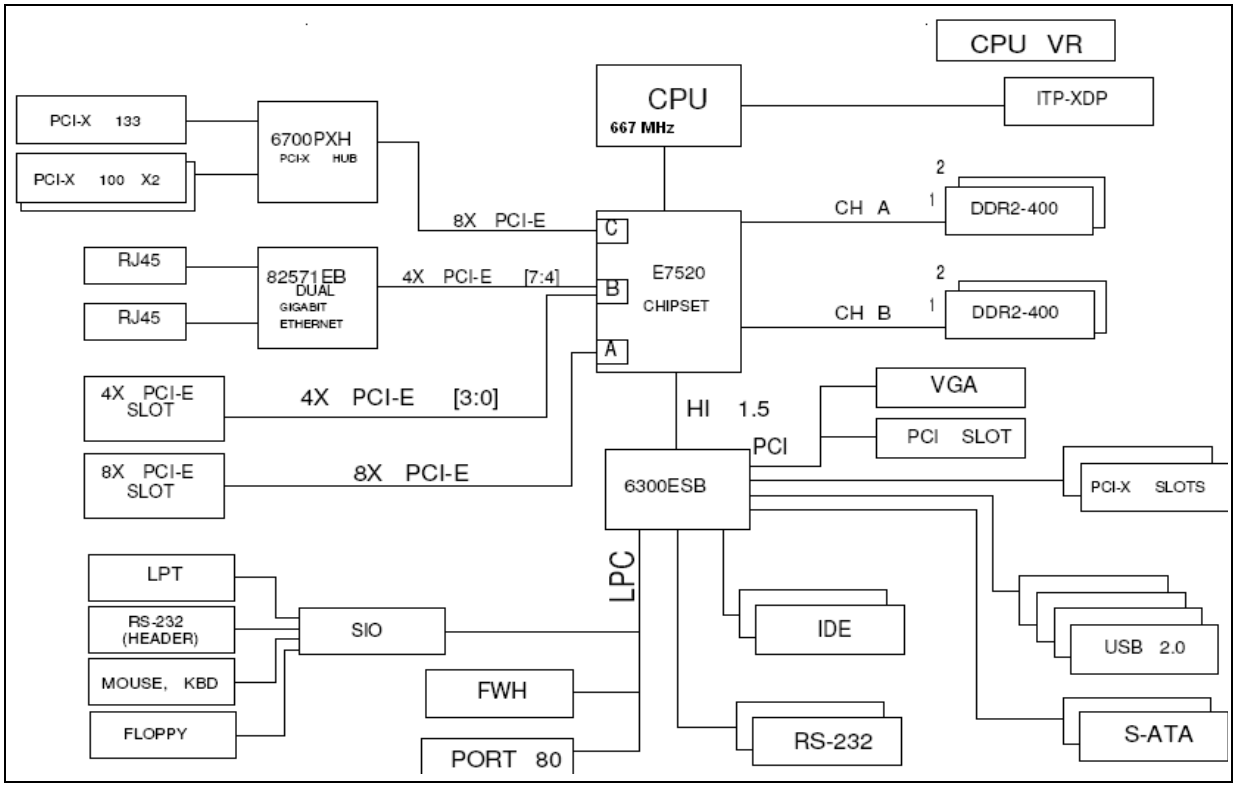
- Move CMOS clear jumper J5H2 to position 2-3 (Configure) for 15 seconds
- Move CMOS clear jumper J5H2 back to position 1-2 (Normal)
- Apply power to the system
- Enter BIOS setup program to set date/time

Note: To avoid damaging the FWH, use an extraction tool such as the AMP822154-1. This tool is not provided with the DEV KIT.

3.0 Theory of Operation

3.1 Block Diagram

Figure 13. Block Diagram of Layout



3.2 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits may be expected to meet their specified performance requirements. Operation outside the functional limit may degrade system performance and cause reliability problems. The development kit shipped with heatsink thermal solution to be installed on the processor. This thermal solution has been tested in an open air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.3 System Features

Processor

- Supports the Intel® Core™ 2 Duo Processor and the Intel® Core™ Duo Processor
- On-board processor voltage regulators compatible with IMVP-6 Design Guide.

Chipset

- Intel® E7520 MCH
- Intel® 6300ESB ICH
- Intel® 6700PXH PCI Hub
- Intel® 82571EB Gigabit Ethernet Controller

Clocking

- CK409B clock synthesizer that generates all host clock and the PCI Express* interface clock for the MCH PHY layer
- DB800 generates the PCI Express differential pair clocks to the onboard PCI Express components and the dedicated PCI Express slots

Memory

- Registered ECC DDR2-400 DIMMs
- Each of the two memory channels on the Intel® E7520 MCH on this evaluation board supports a maximum of two DDR2-400 DIMMs per channel
- 3.2 Gbytes/s bus per channel bandwidth with DDR2-400

Graphics

- ATI Rage Mobility-M graphics controller

I/O

- From Intel® 6300ESB ICH
  - 1 PCI 2.2 32/33 Slot
  - 2 PCI-X 66 MHz slots
  - 2 IDE connectors
  - 2 Serial ATA connectors
  - 2 Serial ports
  - 4 USB 2.0 ports
    Two on rear panel I/O
    Two on front panel header
  - Super I/O via LPC bus from the 6300ESB
    One Floppy port
    One Parallel port
    One Serial port (10-pin header)
    Two PS2 port
- Intel® 6700PXH PCI Hub
  - 2 PCI-X 100 MHz slots
  - 1 PCI-X 133 MHz slot
- Intel® 82571EB Gigabit Ethernet Controller
  - 2 Gigabit Ethernet connections

— X4 PCIe interface with MCH providing bandwidth up to 2 GB/s per direction

— Integrated PHY layer for 10/100/1000 Mbps operation

Low Pin Count Bus

- Super I/O IC
- Firmware hub

Board Form Factor

- 13″ x 16″ for bench top use
- ATX SSI 12 V Power supply

3.3.1 Intel® Core™ 2 Duo Processor

- 2 high performance execution cores at 2.16 GHz on 65nm process technology
- 667 MHz FSB

3.3.2 Intel® Core™ Duo Processor

- 2 high performance execution cores at 2 GHz on 65nm process technology
- 667 MHz FSB

3.3.3 Intel® E7520 MCH

The architecture of the MCH provides the performance and feature set required for Intel® Core™ Duo Processor and Intel® Core™ 2 Duo Processor-based volume to performance servers. Configuration options facilitate optimization of the platform for workloads characteristic of communication, presentation, storage, performance computation, or database applications. Coverage includes the MCH interface units (system bus, system memory, PCI Express, Hub Interface (HI), SMBus, power management, MCH clocking, MCH system reset and power sequencing) as well as RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features.

Features:

- Registered ECC DDR2-400 DIMM support
- Integrated four-channel DMA engine with IOxAPIC functionality
- High speed serial PCI Express interface
- Hub interface to Intel® 6300ESB ICH
- Intel® 6700PXH PCI Hub is a PCIe to PCI-X Hub interface

3.3.4 Intel® 6300ESB ICH

The Intel® 6300ESB ICH is designed for a variety of processors/memory controller hubs. The Intel® 6300ESB ICH provides the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance.

Features:

- Upstream HI for access to the MCH
- Two port Serial ATA controllers
- Two IDE connectors
- PCI-X 1.0 Interface

- PCI 2.2 Interface
- Two serial I/O ports
- Two-stage WDT (Watch Dog Timer)
- LPC Interface
- EPLD for Port 80 decode and display
- FWH Interface
- SMBus 2.0 controller
- I/O APIC
- Four USB 2.0 Ports

3.3.5 Intel® 6700PXH PCI Hub

The 6700PXH provides a connection between the E7520 and PCI or PCI-X interfaces via a PCIe channel. The 6700PXH PCI Hub contains two PCI bus interfaces that have been configured to PCI-X 133 MHz and the other to PCI-X 100 MHz, for either 32-bit or 64-bit PCI devices.

- Two PCI-X 100 MHz slots
- One PCI-X 133 MHz slot

3.3.6 Intel® 82571EB Gigabit Ethernet Controller

The Intel 82571EB Gigabit Ethernet Controller is a single, compact component with two fully integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) ports. Uses the PCI Express X4 connection to the Intel® E7520 MCH. The Intel 82571EB provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

3.3.7 Memory Subsystem

The memory subsystem is designed to support Double Data Rate 2 (DDR2) Synchronous Dynamic Random Access Memory (SDRAM) using the Intel® E7520 MCH. The MCH provides two independent DDR channels, which support DDR2-400 DIMMs. The peak bandwidth of each DDR2 branch channel is 3.2 GByte/s (8 bytes x 400 MT/s) with DDR2-400. When the two DDR2 channels from the MCH operate in lock step, the effective overall peak bandwidth of the DDR2 memory subsystem is 6.4 GByte/s for DDR2-400.

3.3.8 Supported DIMM Module Types

Table 6 shows all DIMM technology validated by Intel on the evaluation board.

Table 6. Supported DIMM Module Types

A1	256 M SR	512 M DR		1 G SR	1 G SR
A2	256 M SR	512 M DR		1 G SR	1 G SR
B1	256 M SR		512 M DR		1 G SR
B2	256 M SR		512 M DR		1 G SR
Size	1 G	1 G	1 G	2 G	4 G
Channels	Dual	Single	Single	Single	Dual

Note: SR = Single Rank; DR = Dual Rank

3.3.9 Memory Population Rules and Configurations

The system supports two DDR2-400 DIMM slots for Channel A and two DDR2-400 DIMM slots for Channel B. The four slots are interleaved and placed in a row in the following order: A1, B1, A2, B2 with A1 being closest to the MCH. This design supports only registered ECC-enabled DIMMs.

When populating both channels, always place identical DIMMs in sockets that have the same position on Channel A and Channel B (i.e., DIMM A2 should be identical to DIMM B2). Refer to datasheet for definition of identical DIMMs.

In addition, single-rank DIMMs should be populated furthest from the MCH when a combination of single-rank and double-rank DIMMs are used. This recommendation is based on the signal integrity requirements of the DDR2 interface.

Figure 14. DDR2-400 Memory—DIMM Ordering

3.3.10 Firmware Hub (FWH)

A socketed FLASH device is used to store system BIOS as well as an Intel® Random Number Generator (RNG). A bootblock locking jumper is provided to allow a mechanical means of protecting the bootblock BIOS firmware. All BIOS programming is controlled via software.

FWH Features:

- 32-pin PLCC package
- Symmetrically-blocked flash memory array (64 Kbyte)
- Pin and register-based block locking
- Integrated hardware RNG
- Single-byte read/write
- Five GPIs

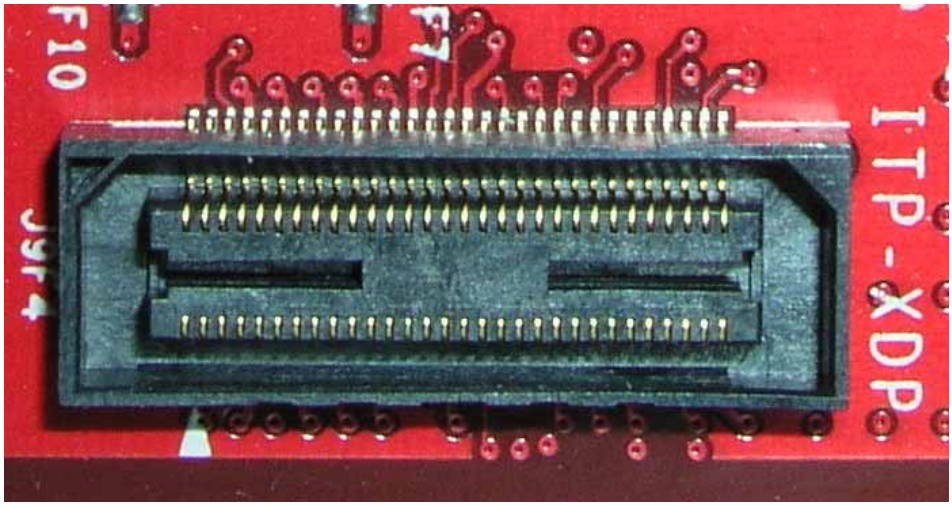
3.3.11 Boot ROM

The system boot ROM is installed on a FWH device. The FWH is addressable on the LPC bus off the Intel® 6300ESB ICH.

3.3.12 In-Target Probe (ITP)

The evaluation board contains an in-target probe (ITP) connector for an ITP-XDP connector. Other ITPs will not work and if installed, could damage the platform and/or the ITP. Figure 15 shows the ITP connector which is located at location J9G1.

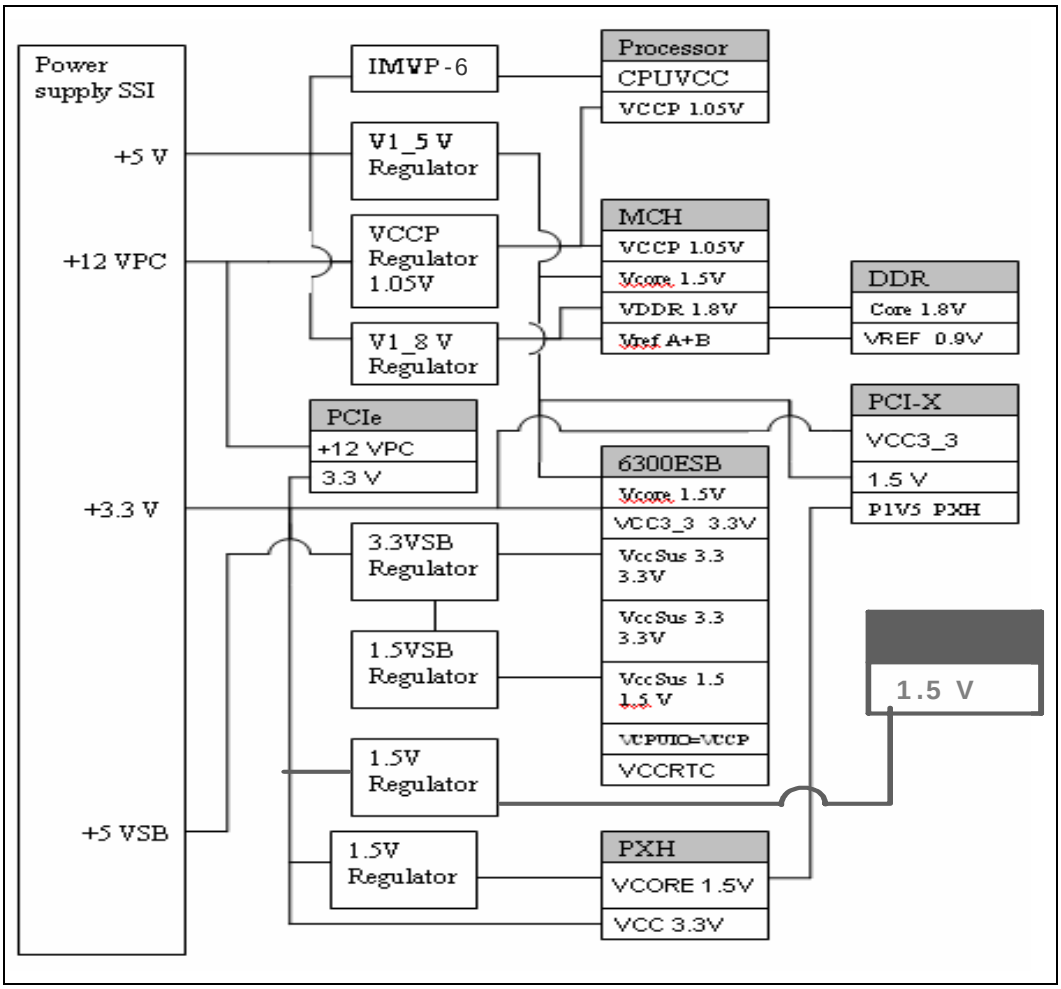
Figure 15. ITP location



3.3.13 Power Diagram

Figure 16 shows the power distribution for the evaluation board. Refer to the evaluation board schematics for details on the power distribution logic (contact your Intel field sales representative to obtain the schematics).

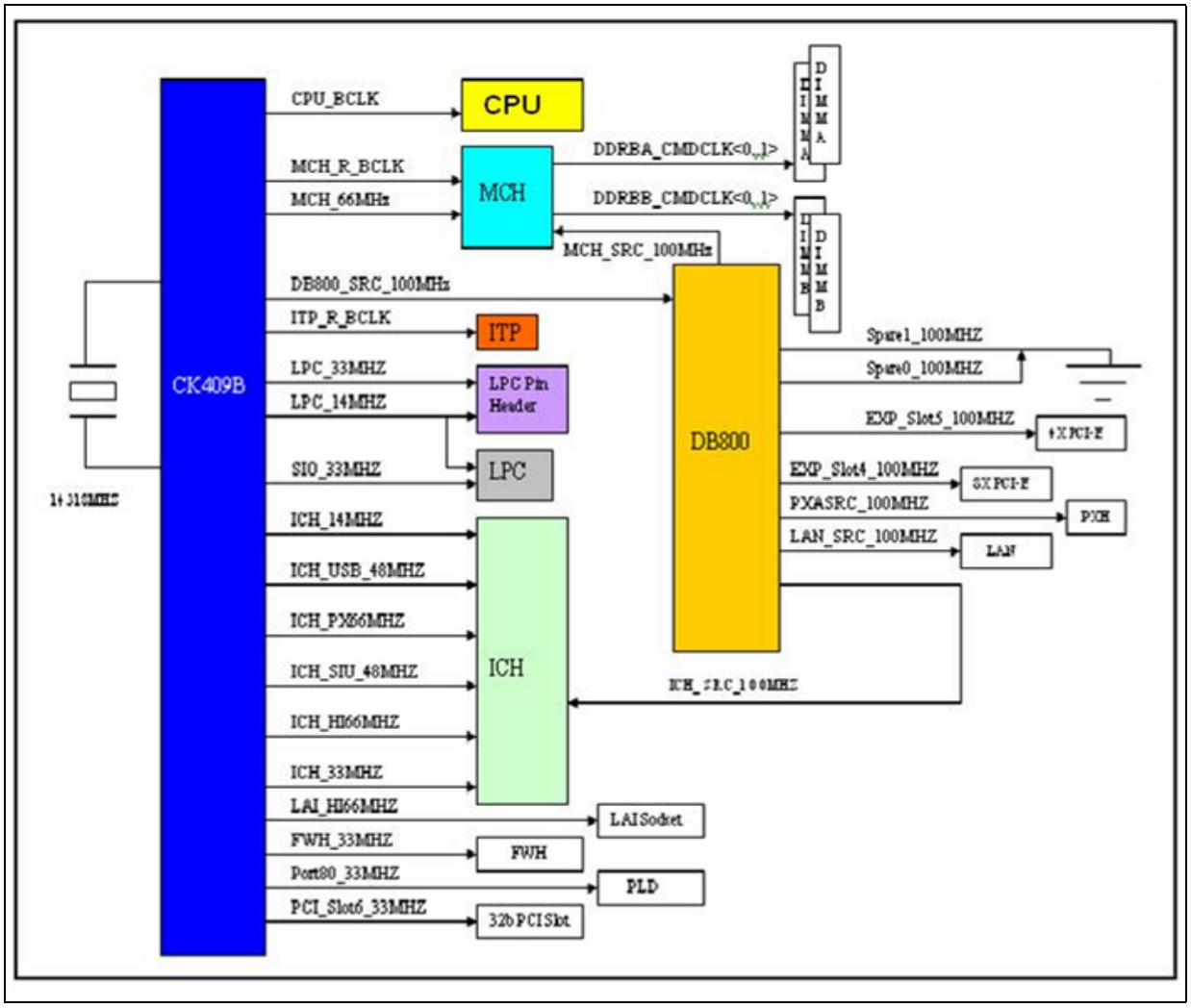
Figure 16. Power Distribution Block Diagram



3.3.14 Clock Generation

The evaluation board uses one CK409B Clock Synthesizer to generate the host differential pair clocks and the 100 MHz differential clock to the DB800. The DB800 then generates the 100 MHz differential pair clock for the PCI Express devices. Figure 17 shows the evaluation board clock configuration.

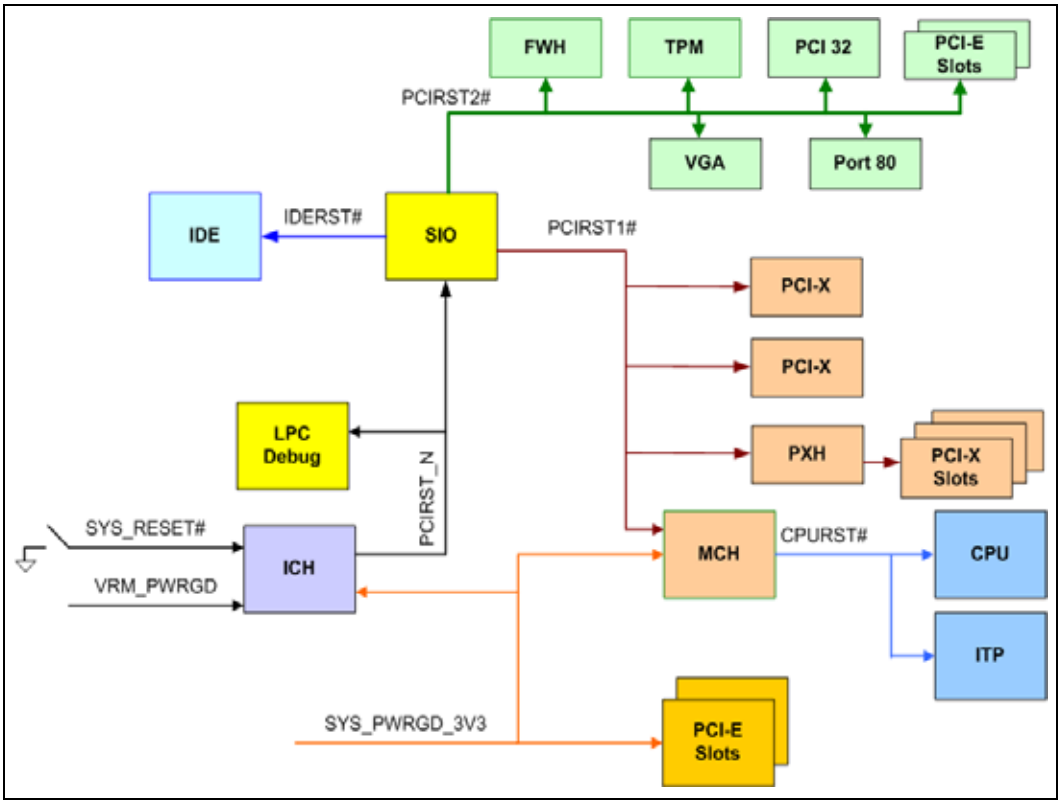
Figure 17. Clock Block Diagram



3.3.15 Platform Resets

Figure 18 depicts the reset logic for the evaluation board. The 6300ESB provides most of the reset, following assertion of power good and system reset.

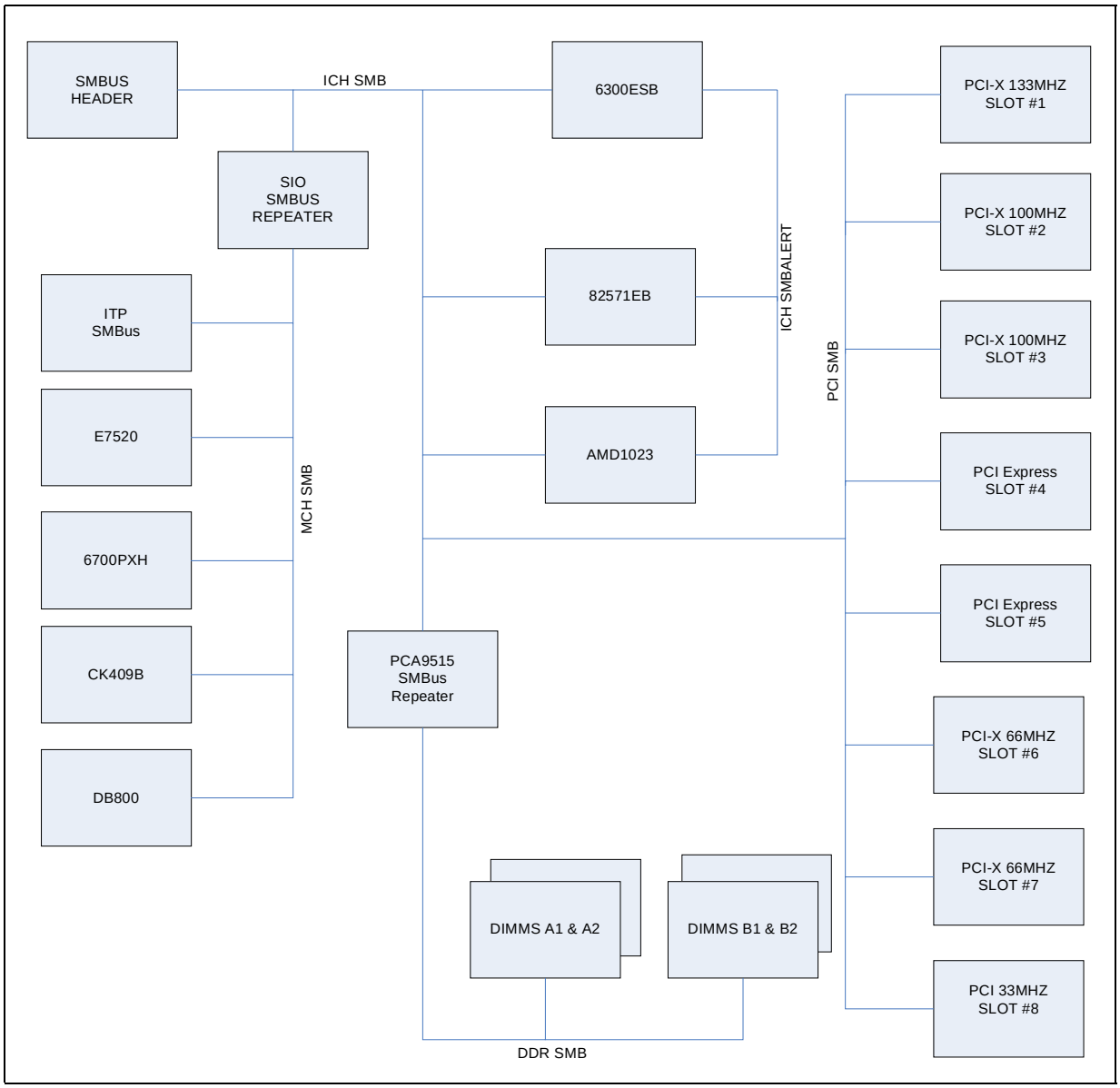
Figure 18. Platform Reset Diagram



3.3.16 SMBus

Figure 19 below illustrates the routing of the SMBus signal among the components.

Figure 19. SMBus Block Diagram

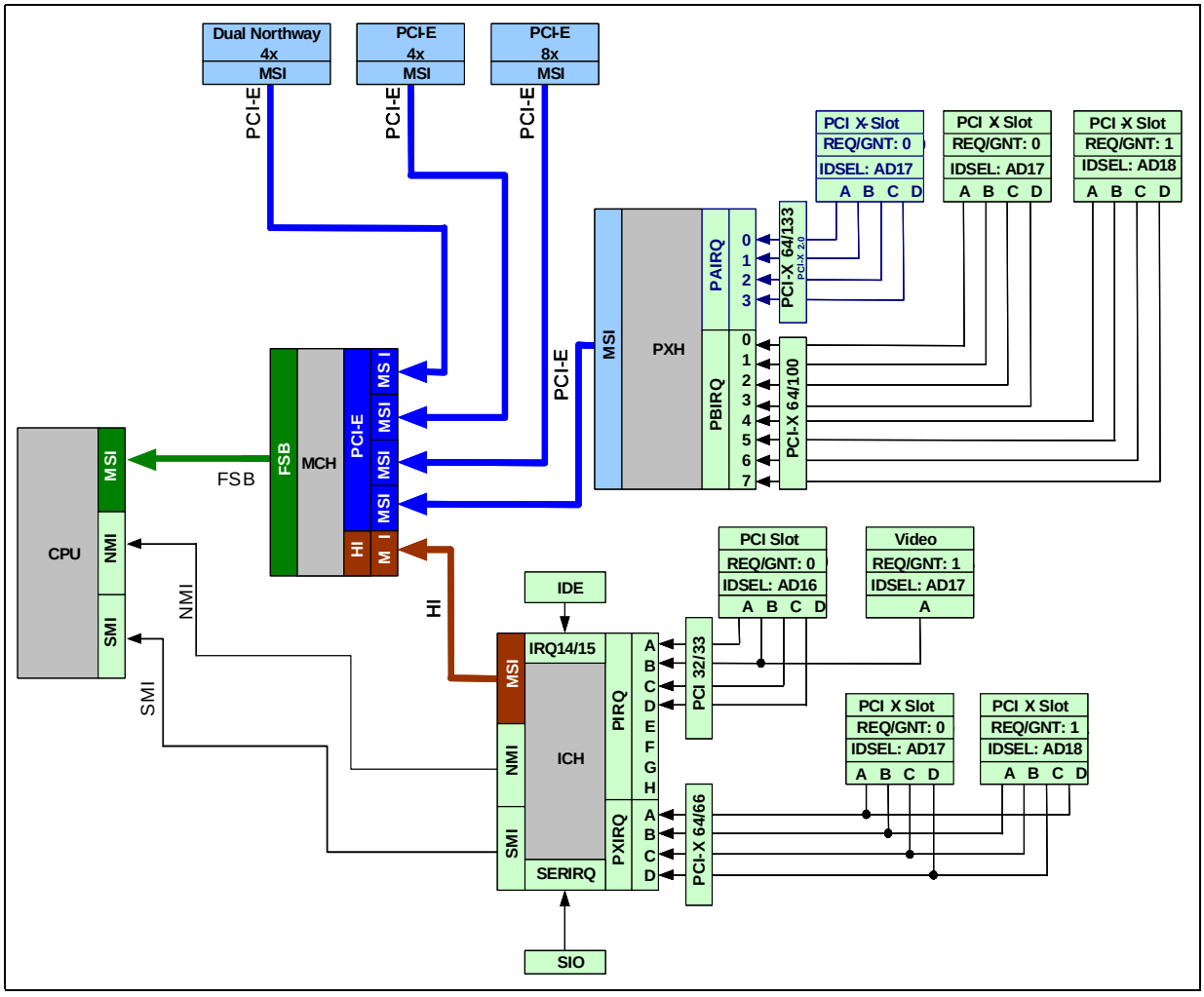


3.3.17 Platform IRQ Routing

Figure 20 shows how the Intel® 6300ESB ICH uses these segments:

- IRQ 14 and 15 for IDE segment
- SERIRQ for SIOPIXRQ segment
- PCRIRQ for the PCI-X segment
- PIRQ for the PCI 32/33 segment

Figure 20. IRQ Routing Diagram



3.3.18 VRD VID Headers

VID headers provide for manual control of the processor core voltage regulator output level(s). Normally, the processor should be run at its default VID (voltage identification) value as set during manufacturing. However, in the event the user needs to set a different VID value from the default value, it can be accomplished through a jumper block found on the board.

Note: These headers are not populated by default. IMVP-6 Controller VID input 0 and 6 are tied low. Initial boards will not have the VID Header populated, processor must have VID override enabled for the initial Intel® Core™ Duo Processor and Intel® Core™ 2 Duo Processor samples. The, VID override enable, jumper controls whether or not the VID header jumpers control the VID to the regulator or not. [1]

1. For the table below 1 means the jumper is installed.

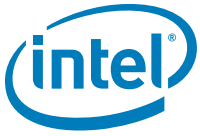
Table 7. Processor VRD Settings

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc-core	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc-core
0	0	0	0	0	0	0	1.5000V	1	0	0	0	0	0	0	0.7000V
0	0	0	0	0	0	1	1.4875V	1	0	0	0	0	0	1	0.6875V
0	0	0	0	0	1	0	1.4750V	1	0	0	0	0	1	0	0.6750V
0	0	0	0	0	1	1	1.4625V	1	0	0	0	0	1	1	0.6625V
0	0	0	0	1	0	0	1.4500V	1	0	0	0	1	0	0	0.6500V
0	0	0	0	1	0	1	1.4375V	1	0	0	0	1	0	1	0.6375V
0	0	0	0	1	1	0	1.4250V	1	0	0	0	1	1	0	0.6250V
0	0	0	0	1	1	1	1.4125V	1	0	0	0	1	1	1	0.6125V
0	0	0	1	0	0	0	1.4000V	1	0	0	1	0	0	0	0.6000V
0	0	0	1	0	0	1	1.3875V	1	0	0	1	0	0	1	0.5875V
0	0	0	1	0	1	0	1.3750V	1	0	0	1	0	1	0	0.5750V
0	0	0	1	0	1	1	1.3625V	1	0	0	1	0	1	1	0.5625V
0	0	0	1	1	0	0	1.3500V	1	0	0	1	1	0	0	0.5500V
0	0	0	1	1	0	1	1.3375V	1	0	0	1	1	0	1	0.5375V
0	0	0	1	1	1	0	1.3250V	1	0	0	1	1	1	0	0.5250V
0	0	0	1	1	1	1	1.3125V	1	0	0	1	1	1	1	0.5125V
0	0	1	0	0	0	0	1.3000V	1	0	1	0	0	0	0	0.5000V
0	0	1	0	0	0	1	1.2875V	1	0	1	0	0	0	1	0.4875V
0	0	1	0	0	1	0	1.2750V	1	0	1	0	0	1	0	0.4750V
0	0	1	0	0	1	1	1.2625V	1	0	1	0	0	1	1	0.4625V
0	0	1	0	1	0	0	1.2500V	1	0	1	0	1	0	0	0.4500V
0	0	1	0	1	0	1	1.2375V	1	0	1	0	1	0	1	0.4375V
0	0	1	0	1	1	0	1.2250V	1	0	1	0	1	1	0	0.4250V
0	0	1	0	1	1	1	1.2125V	1	0	1	0	1	1	1	0.4125V
0	0	1	1	0	0	0	1.2000V	1	0	1	1	0	0	0	0.4000V
0	0	1	1	0	0	1	1.1875V	1	0	1	1	0	0	1	0.3875V
0	0	1	1	0	1	0	1.1750V	1	0	1	1	0	1	0	0.3750V
0	0	1	1	0	1	1	1.1625V	1	0	1	1	0	1	1	0.3625V
0	0	1	1	1	0	0	1.1500V	1	0	1	1	1	0	0	0.3500V
0	0	1	1	1	0	1	1.1375V	1	0	1	1	1	0	1	0.3375V
0	0	1	1	1	1	0	1.1250V	1	0	1	1	1	1	0	0.3250V
0	0	1	1	1	1	1	1.1125V	1	0	1	1	1	1	1	0.3125V
0	1	0	0	0	0	0	1.1000V	1	1	0	0	0	0	0	0.3000V
0	1	0	0	0	0	1	1.0875V	1	1	0	0	0	0	1	0.2875V
0	1	0	0	0	1	0	1.0750V	1	1	0	0	0	1	0	0.2750V
0	1	0	0	0	1	1	1.0625V	1	1	0	0	0	1	1	0.2625V
0	1	0	0	1	0	0	1.0500V	1	1	0	0	1	0	0	0.2500V
0	1	0	0	1	0	1	1.0375V	1	1	0	0	1	0	1	0.2375V
0	1	0	0	1	1	0	1.0250V	1	1	0	0	1	1	0	0.2250V
0	1	0	0	1	1	1	1.0125V	1	1	0	0	1	1	1	0.2125V
0	1	0	1	0	0	0	1.0000V	1	1	0	1	0	0	0	0.2000V
0	1	0	1	0	0	1	0.9875V	1	1	0	1	0	0	1	0.1875V
0	1	0	1	0	1	0	0.9750V	1	1	0	1	0	1	0	0.1750V
0	1	0	1	0	1	1	0.9625V	1	1	0	1	0	1	1	0.1625V
0	1	0	1	1	0	0	0.9500V	1	1	0	1	1	0	0	0.1500V
0	1	0	1	1	0	1	0.9375V	1	1	0	1	1	0	1	0.1375V
0	1	0	1	1	1	0	0.9250V	1	1	0	1	1	1	0	0.1250V
0	1	0	1	1	1	1	0.9125V	1	1	0	1	1	1	1	0.1125V
0	1	1	0	0	0	0	0.9000V	1	1	1	0	0	0	0	0.1000V
0	1	1	0	0	0	1	0.8875V	1	1	1	0	0	0	1	0.0875V
0	1	1	0	0	1	0	0.8750V	1	1	1	0	0	1	0	0.0750V
0	1	1	0	0	1	1	0.8625V	1	1	1	0	0	1	1	0.0625V
0	1	1	0	1	0	0	0.8500V	1	1	1	0	1	0	0	0.0500V
0	1	1	0	1	0	1	0.8375V	1	1	1	0	1	0	1	0.0375V
0	1	1	0	1	1	0	0.8250V	1	1	1	0	1	1	0	0.0250V
0	1	1	0	1	1	1	0.8125V	1	1	1	0	1	1	1	0.0125V
0	1	1	1	0	0	0	0.8000V	1	1	1	1	0	0	0	0.0000V
0	1	1	1	0	0	1	0.7875V	1	1	1	1	0	0	1	0.0000V
0	1	1	1	0	1	0	0.7750V	1	1	1	1	0	1	0	0.0000V
0	1	1	1	0	1	1	0.7625V	1	1	1	1	0	1	1	0.0000V
0	1	1	1	1	0	0	0.7500V	1	1	1	1	1	0	0	0.0000V
0	1	1	1	1	0	1	0.7375V	1	1	1	1	1	0	1	0.0000V
0	1	1	1	1	1	0	0.7250V	1	1	1	1	1	1	0	0.0000V
0	1	1	1	1	1	1	0.7125V	1	1	1	1	1	1	1	0.0000V

3.4 Battery Requirements

A type 2032 3 V lithium coin cell battery is required and included in the evaluation board kit.

Warning: Risk of explosion if the lithium battery is replaced by an incorrect type. Ensure the correct type of battery is selected and installed correctly before turning power on to the board.



4.0 Platform Management

The following sections describe how the system power management operates, and how the different ACPI states are implemented. Platform management involves:

- ACPI implementation-specific details
- System monitoring, control, and response to thermal, voltage, and intrusion events
- BIOS security

4.1 Power Button

The system power button is connected to the I/O controller component. When the button is pressed, the I/O controller receives the signal and transitions the system to the proper sleep state as determined by the operating system and software. If the power button is pressed and held for four seconds, the system powers off (S5 state). This feature is called power button override and is particularly helpful in case of system hang and system lock. The power button is located at location SW3E1on the board.

4.2 Sleep States Supported

The I/O controller controls the system sleep states. States S0, S1, S3, and S5 are supported. The platform enters sleep states in response to BIOS, operating system, or user actions. Normally the operating system determines which sleep state to transition into. However, a four second power button override event places the system immediately into S5. When transitioning into a software-invoked sleep state, the I/O controller attempts to gracefully put the system to sleep by first going into the processor C2 state.

4.2.1 S0 State

This is the normal operating state, even though there are some power savings modes in this state using processor Halt and Stop Clock (processor C1 and C2 states). S0 affords the fastest wake-up response time of any sleep state because the system remains fully powered and memory is intact.

4.2.2 S1 State

This state is entered via a processor Sleep signal from the I/O controller (processor C3 state). The system remains fully powered with memory contents intact but the processors enter their lowest power state. Wake-up latency is slightly longer in this state than in S0; however, power savings are improved from S0.

4.2.3 S2 State

This state is not supported.

4.2.4 S3 State

This state is called Suspend to RAM (STR). The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except the RTC. S3 is entered when the I/O controller asserts the SLP_S3# signal to downstream circuitry to control 1.8 V power plane switching. Power must be switched from the normal 1.8 V rail to standby 1.8 V, because the 450 W SSI 12 V power supply does not directly supply a standby 1.8 V rail. The sequence to enter Suspend to RAM is as follows:

1. The OS and BIOS prepare for S3 sleep state.
2. The OS sets the appropriate sleep bits in the I/O controller.
3. The I/O controller drives STPCLK to the processor.
4. The processor respond with a Stop-Grant cycle, passed over hub interface by MCH.
5. The I/O controller indicates an S3 (STR) sleep mode to the MCH via Hub Interface A.
6. The MCH puts DDR memory into the self-refresh mode.
7. The MCH drives DDR CMDCLK differential pairs and all DDR outputs low.
8. The MCH drives a completion message via Hub Interface A to the I/O controller.
9. The I/O controller turns off all voltage rails (except Standby 5 V) from the main power supply by asserting the SLP_S3_N signal.

When in the S3 state, only the standby 5 V rail is available from the power supply. The board uses this standby source to generate 1.8 V standby rail to power the DIMMs.

The asserted SLP_S3_N signal also controls the logic to switch the DIMM power source from main 1.8 V to standby 1.8 V.

4.2.5 S4 State

This state is not supported.

4.2.6 S5 State

This state is the normal off state whether entered through the power button or soft off. All power is shut off except for the logic required to restart. The system remains in the S5 state only while the power supply is plugged into the electrical outlet. If the power supply is unplugged, this is considered a mechanical off or G3.

4.2.7 Wake-Up Events

The types of wake-up events and wake-up latencies are related to the actual power rails available to the system in a particular sleep state, as well as to the location in which the system context is stored. Regardless of the sleep state, wake on the power button is always supported except in a mechanical off situation. When in a sleep state, the system complies with the PCI specification by supplying the optional 3.3 V standby voltage to each PCI slot as well as the PME# signal. This enables any compliant PCI card to wake up the system from any supported sleep state except mechanical off.

4.2.8 Wake from S1 Sleep State

During S1 the system is fully powered, permitting support for PCI Express* Wake and Wake on PCI PME#.

4.2.9 Wake from S3 State

Keyboard press or mouse movement is used to wake from S3.

4.2.10 Wake from S5 State

The power button is used to wake from S5.

4.3 PCI PM Support

This design holds the system reset signal low when in a sleep state. The system supports the PCI PME# signal and provides 3.3 V standby to the PCI and PCI Express slots. This support allows any compliant PCI or PCI Express card to wake up the system from any sleep state except mechanical off. Because of the limited amount of power available on 3.3 V standby, the user and the operating system must configure the system carefully following the PCI power management interface specification.

4.4 Platform Management

The ADM1023 monitors the majority of the system voltages. All voltage levels can be read via the SMBus.

4.4.1 Processor Thermal Management

Each processor monitors its own core temperature and thermally manages itself when it reaches a certain temperature. The system also uses the internal processor diode to monitor the die temperature. The diode pins are routed to the diode input pins in the ADM1023. The ADM1023 will use its A/D converter to determine the CPU temperature. When the CPU temperature reaches its threshold, System Management will react accordingly to lower the overall system temperature.

4.5 System Fan Operation

Power consumption can be adjusted by controlling the fan speed. The fan can be off, running on 5 V, or running on 12 V. The system can adjust the fan speed depending on the CPU temperature. If a system gets too hot, an alert will be sent to the System Management controller. The administrator may then want to turn the system off but keep the fan running to cool the system faster.

5.0 Driver and Operating System Support

The development kit supports the following operating systems:

- Red Hat* EL 3.0 AS and WS
- QNX Neutrino*
- Microsoft Windows Server 2003*
- Microsoft Windows XP* and embedded XP*

Note: Operating systems are not included in the development kit.

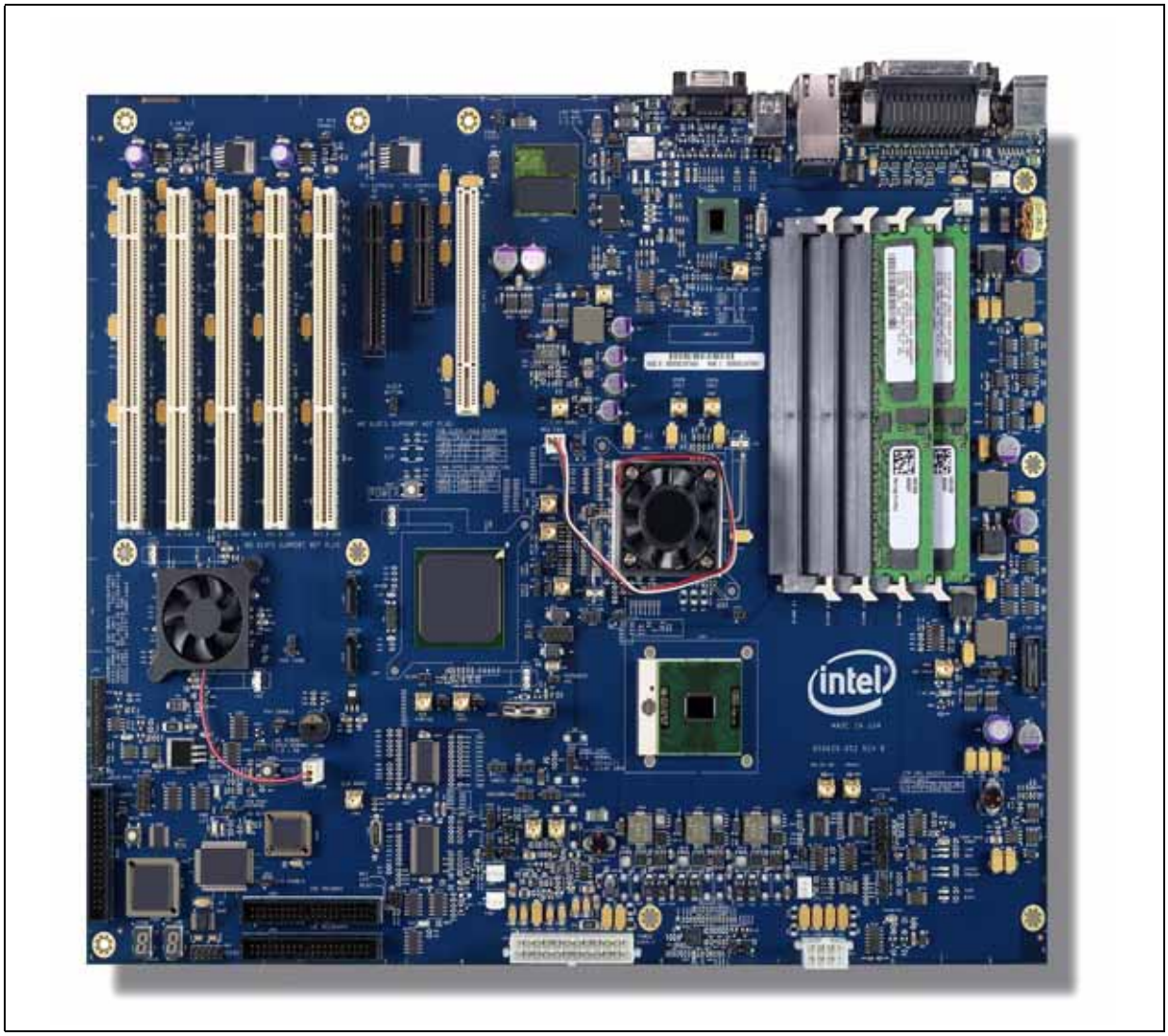
5.1 Video Driver Issue

The ATI video software driver included with this development kit does not fully comply with the new guidelines set forth in the software developer's manual (SDM), chapter 10. This section outlines the utilization of memory cache control. You may experience infrequent issue when resuming from a S3 state. There should be no other issues with this software video driver.

6.0 Hardware Reference

This section provides reference information on the hardware, including locations of evaluation board components, connector pinout information, and jumper settings. Figure 21 shows the evaluation board.

Figure 21. Evaluation Board



6.1 Chipset Components

Table 8 lists the chipset and other major components on the evaluation board.

Table 8. Chipset Components

Component Designator	Component Description
U6E1	Intel® E7520 Memory Controller Hub (MCH)
U4F1	Intel® 6300ESB I/O Controller Hub (ICH)
U2F1	Intel® 6700PXH PCI Hub
U6B1	Intel® 82571EB Gigabit Ethernet Controller
U2H3	Firmware Hub (FWH)

6.2 Expansion Slots and Sockets

Table 9 lists the expansion slots and sockets on the evaluation board.

Table 9. Expansion Slots and Socket

Slot/Socket Reference Designator	Slot/Socket Description
J3B2	PCI Express* Port A (x8)
J4B2	PCI Express* Port B (x4)
J4B1	PCI Slot
J1B1	PCI-X Slot (PXH)
J1B2	PCI-X Slot (PXH)
J2B1	PCI-X Slot (PXH)
J2B2	PCI-X Slot (ICH)
J3B1	PCI-X Slot (ICH)
U6G1	Processor
XB5G1	Battery

6.2.1 PCI Express* Connector

Table 10 lists the signals assigned to the PCI Express port A slot connector found at J3B2.

Table 10. PCI Express* Port A (x8) Connector Pinout (Sheet 1 of 2)

Pin	Signal	Pin	Signal
A1	PRSNT1#	B1	12 V
A2	12 V	B2	12 V
A3	12 V	B3	12 V
A4	GND	B4	GND
A5	JTAG2	B5	SMCLK
A6	JTAG3	B6	SMDAT
A7	JTAG4	B7	GND
A8	JTAG5	B8	3.3 V
A9	3.3 V	B9	JTAG1

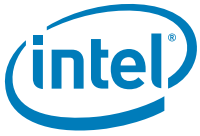


Table 10. PCI Express* Port A (x8) Connector Pinout (Sheet 2 of 2)

Pin	Signal	Pin	Signal
A10	3.3 V	B10	3.3 V_{AUX}
A11	PWRGD	B11	WAKE#
A12	GND	B12	Reserved
A13	Refclk+	B13	GND
A14	Refclk -	B14	HSOP_0
A15	GND	B15	HSON_0
A16	HSIP_0	B16	GND
A17	HSIN_0	B17	PRSNT2_1#
A18	GND	B18	GND
A19	Reserved	B19	HSOP_1
A20	GND	B20	HSON_1
A21	HSIP_1	B21	GND
A22	HSIN_1	B22	GND
A23	GND	B23	HSOP_2
A24	GND	B24	HSON_2
A25	HSIP_2	B25	GND
A26	HSIN_2	B26	GND
A27	GND	B27	HSOP_3
A28	GND	B28	HSON_3
A29	HSIP_3	B29	GND
A30	HSIN_3	B30	Reserved
A31	GND	B31	PRSNT2_2#
A32	Reserved	B32	GND
A33	Reserved	B33	HSOP_4
A34	GND	B34	HSON_4
A35	HSIP_4	B35	GND
A36	HSIN_4	B36	GND
A37	GND	B37	HSOP_5
A38	GND	B38	HSON_5
A39	HSIP_5	B39	GND
A40	HSIN_5	B40	GND
A41	GND	B41	HSOP_6
A42	GND	B42	HSON_6
A43	HSIP_6	B43	GND
A44	HSIN_6	B44	GND
A45	GND	B45	HSOP_7
A46	GND	B46	HSON_7
A47	HSIP_7	B47	GND
A48	HSIN_7	B48	PRSNT2_3#
A49	GND	B49	GND

Table 11 lists the signals assigned to the PCI Express Port B slot connector found at J4B2.

Table 11. PCI Express* Port B (X4) Connector Pinout

Pin	Signal	Pin	Signal
A1	PRSNT1#	B1	12 V
A2	12 V	B2	12 V
A3	12 V	B3	12 V
A4	GND	B4	GND
A5	JTAG2	B5	SMCLK
A6	JTAG3	B6	SMDAT
A7	JTAG4	B7	GND
A8	JTAG5	B8	3.3 V
A9	3.3 V	B9	JTAG1
A10	3.3 V	B10	3.3 V_{AUX}
A11	PWRGD	B11	WAKE#
A12	GND	B12	Reserved
A13	Refclk+	B13	GND
A14	Refclk -	B14	HSOP_0
A15	GND	B15	HSON_0
A16	HSIP_0	B16	GND
A17	HSIN_0	B17	PRSNT2_1#
A18	GND	B18	GND
A19	Reserved	B19	HSOP_1
A20	GND	B20	HSON_1
A21	HSIP_1	B21	GND
A22	HSIN_1	B22	GND
A23	GND	B23	HSOP_2
A24	GND	B24	HSON_2
A25	HSIP_2	B25	GND
A26	HSIN_2	B26	GND
A27	GND	B27	HSOP_3
A28	GND	B28	HSON_3
A29	HSIP_3	B29	GND
A30	HSIN_3	B30	Reserved
A31	GND	B31	PRSNT2_2#
A32	Reserved	B32	GND

6.2.2 32-Bit PCI Connector

Table 12 presents the signals assigned to the 32-bit PCI slot connector found at J4B1.

Table 12. 32-Bit 5 V PCI Connector Pinout (Sheet 1 of 2)

Pin	Signal	Pin	Signal
A1	TRST#	B1	-12 V
A2	+12 V	B2	TCK
A3	TMS	B3	GND
A4	TDI	B4	TDO
A5	5 V	B5	5 V
A6	INTA#	B6	5 V
A7	INTC#	B7	INTB#
A8	5 V	B8	INTD#
A9	RSVD1	B9	PRSNT1#
A10	5 V	B10	Reserved
A11	RSVD3	B11	PRSNT2#
A12	GND	B12	GND
A13	GND	B13	GND
A14	3.3 V_{AUX}	B14	Reserved
A15	RST#	B15	GND
A16	5 V	B16	CLK
A17	GNT#	B17	GND
A18	GND	B18	REQ#
A19	PME#	B19	5 V
A20	AD30	B20	AD31
A21	3.3 V	B21	AD29
A22	AD28	B22	GND
A23	AD26	B23	AD27
A24	GND	B24	AD25
A25	AD24	B25	3.3 V
A26	IDSEL	B26	C/BE3#
A27	3.3 V	B27	AD23
A28	AD22	B28	GND
A29	AD20	B29	AD21
A30	GND	B30	AD19
A31	AD18	B31	3.3 V
A32	AD16	B32	AD17
A33	3.3 V	B33	C/BE2#
A34	FRAME#	B34	GND
A35	GND	B35	IRDY#
A36	TRDY#	B36	3.3 V
A37	GND	B37	DEVSEL#

Table 12. 32-Bit 5 V PCI Connector Pinout (Sheet 2 of 2)

Pin	Signal	Pin	Signal
A38	STOP#	B38	GND
A39	3.3 V	B39	LOCK#
A40	SDONE	B40	PERR#
A41	SBO#	B41	3.3 V
A42	GND	B42	SERR#
A43	PAR	B43	3.3 V
A44	AD15	B44	C/BE1#
A45	3.3 V	B45	AD14
A46	AD13	B46	GND
A47	AD11	B47	AD12
A48	GND	B48	AD10
A49	AD9	B49	GND
A50	KEY	B50	KEY
A51	KEY	B51	KEY
A52	CBEO#	B52	AD8
A53	3.3 V	B53	AD7
A54	AD6	B54	3.3 V
A55	AD4	B55	AD5
A56	GND	B56	AD3
A57	AD2	B57	GND
A58	AD0	B58	AD1
A59	5 V	B59	5 V
A60	REQ64#	B60	ACK64#
A61	5 V	B61	5 V
A62	5 V	B62	5 V

6.2.3 PCI-X Connector

Table 13 presents the PCI-X connector pinout for J1B1, J1B2, J2B1, J2B2, and J3B1.

Table 13. PCI-X Connector Pinout (Sheet 1 of 4)

Pin	Signal	Pin	Signal
A1	TRST#	B1	-12 V
A2	+12 V	B2	TCK
A3	TMS	B3	GND
A4	TDI	B4	TDO
A5	5 V	B5	5 V
A6	INTA#	B6	5 V
A7	INTC#	B7	INTB#
A8	5 V	B8	INTD#
A9	Reserved	B9	PRSNT1#

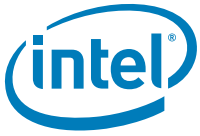


Table 13. PCI-X Connector Pinout (Sheet 2 of 4)

Pin	Signal	Pin	Signal
A10	3.3 V	B10	Reserved
A11	Reserved	B11	PRSNT2#
A12	KEY	B12	KEY
A13	KEY	B13	KEY
A14	3.3 V_{AUX}	B14	Reserved
A15	RST#	B15	GND
A16	3.3 V	B16	CLK
A17	GNT#	B17	GND
A18	GND	B18	REQ#
A19	PME#	B19	3.3 V
A20	AD30	B20	AD31
A21	3.3 V	B21	AD29
A22	AD28	B22	GND
A23	AD26	B23	AD27
A24	GND	B24	AD25
A25	AD24	B25	3.3 V
A26	IDSEL	B26	C/BE3#
A27	3.3 V	B27	AD23
A28	AD22	B28	GND
A29	AD20	B29	AD21
A30	GND	B30	AD19
A31	AD18	B31	3.3 V
A32	AD16	B32	AD17
A33	3.3 V	B33	C/BE2#
A34	FRAME#	B34	GND
A35	GND	B35	IRDY#
A36	TRDY#	B36	3.3 V
A37	GND	B37	DEVSEL#
A38	STOP#	B38	PCIXCAP
A39	3.3 V	B39	LOCK#
A40	SDONE	B40	PERR#
A41	SBO#	B41	3.3 V
A42	GND	B42	SERR#
A43	PAR	B43	3.3 V
A44	AD15	B44	CBE1#
A45	3.3 V	B45	AD14
A46	AD13	B46	GND
A47	AD11	B47	AD12
A48	GND	B48	AD10
A49	AD9	B49	M66EN

Table 13. PCI-X Connector Pinout (Sheet 3 of 4)

Pin	Signal	Pin	Signal
A50	GND	B50	GND
A51	GND	B51	GND
A52	CBEO#	B52	AD8
A53	3.3 V	B53	AD7
A54	AD6	B54	3.3 V
A55	AD4	B55	AD5
A56	GND	B56	AD3
A57	AD2	B57	GND
A58	AD0	B58	AD1
A59	3.3 V	B59	3.3 V
A60	REQ64#	B60	ACK64#
A61	5 V	B61	5 V
A62	5 V	B62	5 V
A63	GND	B63	Reserved
A64	C/BE7#	B64	GND
A65	C/BE5#	B65	C/BE6#
A66	3.3 V	B66	C/BE4#
A67	PAR64	B67	GND
A68	AD62	B68	AD63
A69	GND	B69	AD61
A70	AD60	B70	3.3 V
A71	AD58	B71	AD59
A72	GND	B72	AD57
A73	AD56	B73	GND
A74	AD54	B74	AD55
A75	3.3 V	B75	AD53
A76	AD52	B76	GND
A77	AD50	B77	AD51
A78	GND	B78	AD49
A79	AD48	B79	3.3 V
A80	AD46	B80	AD47
A81	GND	B81	AD45
A82	AD44	B82	GND
A83	AD42	B83	AD43
A84	3.3 V	B84	AD41
A85	AD40	B85	GND
A86	AD38	B86	AD39
A87	GND	B87	AD37
A88	AD36	B88	3.3V
A89	AD34	B89	AD35

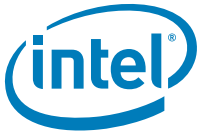


Table 13. PCI-X Connector Pinout (Sheet 4 of 4)

Pin	Signal	Pin	Signal
A90	GND	B90	AD33
A91	AD32	B91	GND
A92	Reserved	B92	Reserved
A93	GND	B93	Reserved
A94	Reserved	B94	GND

6.2.4 Processor Sockets

The processor is keyed so that it fits into the socket in one particular orientation.

6.2.5 Firmware Hub (FWH) BIOS Socket

The system boot ROM is installed on the ATMEL AT49LW080 or SST ST49LF008A Firmware Hub device. The FWH is addressable on the LPC bus off the Intel® 6300ESB ICH.

The FWH or BIOS flash memory fits into the 32-pin socket U2H3, giving you the option to remove and reprogram it without the use of soldering equipment. There is also a flash utility that is supplied with the BIOS that can be used to program the FWH. This is the recommended way to program the FWH.

There is only one correct orientation for the FWH to be placed into its socket. Line up the circular marking on the FWH, denoting pin one, with the arrow marking on the evaluation board socket.

Note: An additional BIOS flash memory is included in the development kit. This BIOS chip must be installed in the platform when the Intel® Core™ Duo Processor is used. See section 2.6 for more details on how to replace the BIOS chip.

6.2.6 Battery

A type 2032, 3 V lithium coin cell battery is used in socket XB5G1 on the evaluation board. The battery is held in place by a metal arm. To remove the battery, gently push the metal arm and remove the battery.

Warning: Risk of explosion if the lithium battery is replaced by an incorrect type. Ensure the correct type of battery is selected and installed correctly before turning power on to the board.

6.3 On-Board Connectors

Table 14. On-Board Connector

Connector Reference Designator	Connector Description
J3F1, J3F2	SATA Connector
J2J2, J2K2	IDE Connectors
J1J1	Floppy Connector
J9G1	ITP Connector
J1H3	Front Panel Connector

6.3.1 SATA Connector

Table 15. SATA Connector Pinout

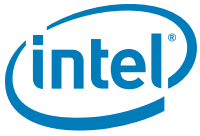
Pin	Connector Description
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	GND

6.3.2 IDE Connector

The evaluation board has two 40-pin connectors for the IDE controllers present in the Intel® 6300ESB ICH. Table 16 lists the signals assigned to the IDE connectors.

Table 16. IDE Connector Pinout

Pin	Connector Description	Pin	Connector Description
1	Reset IDE	21	PDDREQ
2	GND	22	GND
3	Host Data	23	I/O Write#
4	Host Data	24	GND
5	Host Data	25	I/O Read#
6	Host Data	26	GND
7	Host Data	27	I/O CHRDY
8	Host Data	28	GND
9	Host Data	29	DACK#
10	Host Data	30	GND
11	Host Data	31	IRQ14
12	Host Data	32	Reserved
13	Host Data	33	Addr1
14	Host Data	34	Primary IDE Cable Detect
15	Host Data	35	Addr0
16	Host Data	36	Addr2
17	Host Data	37	Chip Select 1#
18	Host Data	38	Chip Select 3#
19	GND	39	Activity
20	Key	40	GND



6.3.3 Floppy Drive Connector

The evaluation board provides one 34-pin floppy connector, which is located at J1J1.

Table 17. Floppy Drive Connector Pinout

Pin	Signal	Pin	Signal
1	GND	18	DIR#
2	Drive Enable 0	19	GND
3	GND	20	STEP#
4	Reserved	21	GND
5	Key	22	Write Data#
6	Drive Enable 1	23	GND
7	GND	24	Write Gate#
8	Index	25	GND
9	GND	26	Track 00#
10	Motor Enable A#	27	GND
11	GND	28	Write Protect#
12	Reserved	29	GND
13	GND	30	Read Data#
14	Drive Select 0#	31	GND
15	GND	32	Side 1 Select#
16	Reserved	33	GND
17	GND	34	Diskette Change#

6.3.4 Front Panel Connector

The development kit is not shipped with a chassis, so the front panel connector is unused by default. However, if you want to place your evaluation board in a chassis, refer to Table 18 for the pinout of the front panel connector J1H3.

Table 18. Front Panel Connector Pinout

Pin	Connector Description	Pin	Connector Description
1	V_{CC}	2	HD_ACT_LED_N
3	No connect	4	FPNTPNL_PWR_LED
5	GND	6	FP_PWR_BTN_N
7	FP_RST_BTN_N	8	GND
9	No connect	10	No Pin

6.4 Jumpers

The evaluation board has a number of jumpers that control various functions of the system.

Table 19 presents the descriptions of the jumpers and their settings.

Figure 22 illustrates the locations of key jumpers on the board.

Table 19. Jumpers and Descriptions

Jumper	Description / Settings	Default Position
J2G3	Enable PXH 1-2: Enable (LH) Open: Disable (LH-VS)	1-2
J2H2	Processor socket occupy signal routing Short: Processor present Open: Processor not present	1-2
J2J1	Enable Super IO chip 1-2: Enable Open: Disable	1-2
J5H2	CMOS clear 1-2: Normal 2-3: Configure	1-2
J7J2	Processor VID override 1-2: Manual select Open: Processor select	Open
J8H3	Processor VID VID[5]: 11-12 VID[4]: 1-2 VID[3]: 3-4 VID[2]: 5-6 VID[1]: 7-8 VID[0]: 9-10	(1.212 V) 1-2 Open 3-4 Open 5-6 Short 7-8 Open 9-10 Open 11-12 Short
J4A1	Enable on-board video 1-2: Enable Open: Disable	1-2
J4H2 (BSEL1), J4J2 (BSEL0)	FSB clock frequency override (J4H2/J4J2/Speed) Open/Open/166 MHz 1-2/1-2/Auto	J4H2: 1-2 J4J2: 1-2
J5F6 (PLLSEL1), J5E3 (PLLSEL0)	DIMM speed configuration (J5F6/J5E3/FSB Freq) Open/Short/667 Open/Short/533	J5E3: 1-2 J5F6: Open
J9G4 (DIMCH), J9G3 (MCH_2)	ITP Processor access (J9G3/J9G4/Mode) 1-2/Open/Processor Access Only 2-3/1-2/Chain Test	J9G3: 1-2 J9G4: Open
J1A1	3.3V AUX switch @ 1.7A 1-2: Enable AUX voltage Open: Disable	1-2
J2G1	For validation only	Open
J2H1	Speaker pull-up routing 1-2: Enable Open: Disable	Open

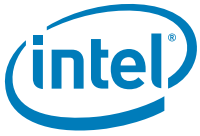


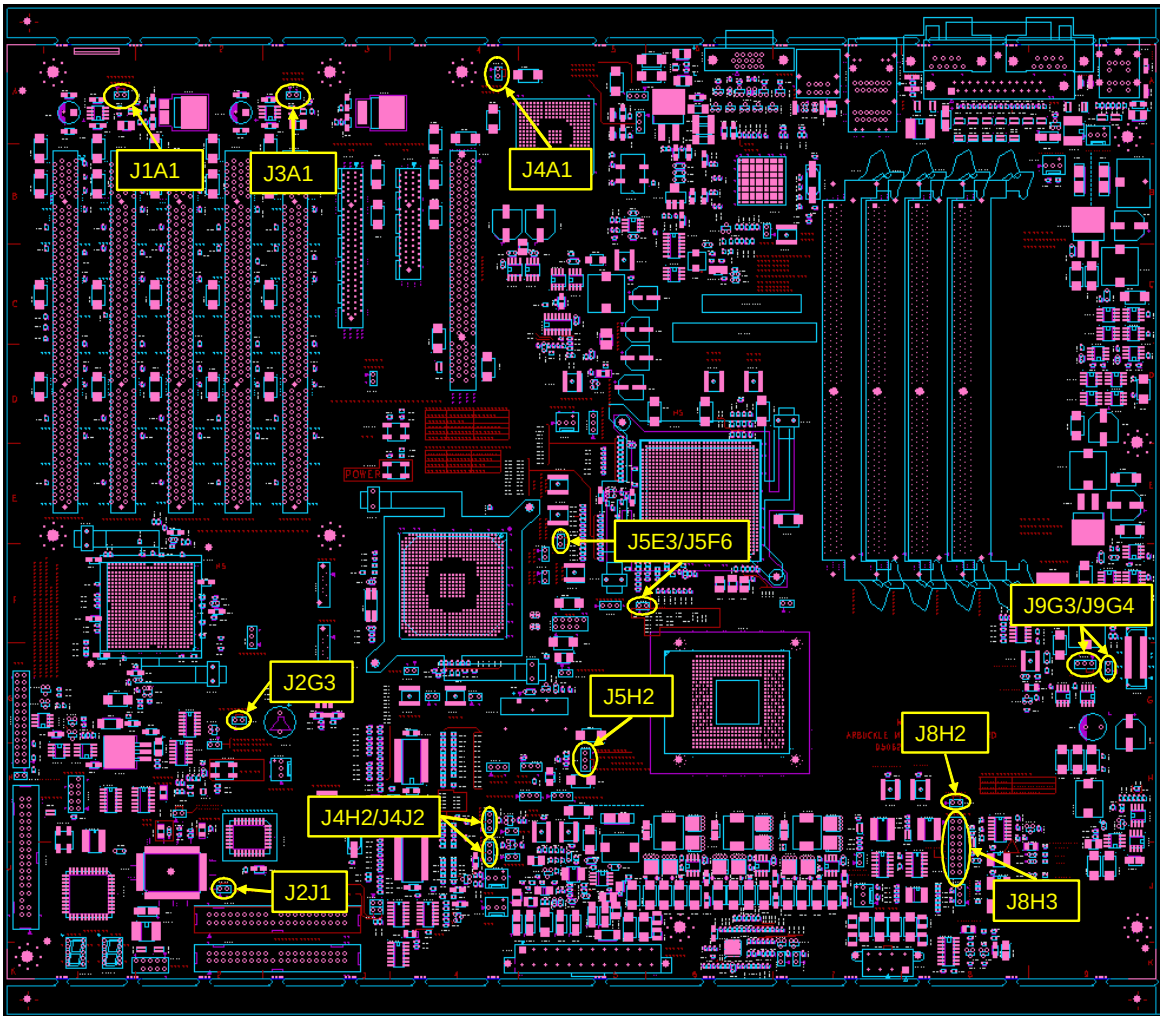
Table 19. Jumpers and Descriptions

Jumper	Description / Settings	Default Position
J3A1	5V AUX switch @ 1.7A 1-2: Enable Open: Disable	1-2
J3D1	Front panel sleep button Open: (For external access only)	Open
J3J1	For validation only	Open
J3J2	For validation only	Open
J4G1	For validation only	Open
J4G4	For validation only	Open
J4G5	For validation only	Open
J4H1	PCI SMB Clock and PCI SMB Data ground 1-2: SMBData grounded 2-3: SMBClk grounded Open: IDLE	Open
J5H1	LAN SMB Clock and LAN SMB Data ground 1-2: SMBData grounded 2-3: SMBClk grounded Open: IDLE	Open
J5H3	DIMM SMB Clock and DIMM SMB Data ground 1-2: SMBData grounded 2-3: SMBClk grounded Open: IDLE	Open
J4H3	For validation only	Open
J4J1	For validation only	Open
J5A1	To manually control LAN_AUXPWR_STRAP either pulled up to 3.3V or pulled down to GND 1-2: Disable 2-3: Enable Open: IDLE	Open
J5D3	MCH SMB Clock and MCH SMB Data ground 1-2: SMBData grounded 2-3: SMBClk grounded Open: IDLE	Open
J5F1	Enable A16 ICH swap override Short: Top Swap Open: Normal	Open
J5F3	Enable ICH run at safe mode Short: Safe Mode Open: Normal	Open
J5F5	For validation only	Open

Table 19. Jumpers and Descriptions

Jumper	Description / Settings	Default Position
J5A1 (3.3V Supply), J5A2 (LAN_AUXPWR_STRAP), J6B1 (ICH_Wake)	LAN Wake On Control (J5A1/J5A2/J6B1/Lan Wake On Status) 1-2/1-2/1-2/Wake On 2-3/2-3/1-2/No Wake On	J5A1: 2-3 J5A2: 2-3 J6B1: 1-2
J8H2	DDR S3 Enable BCKFD_CT_LTCH Short: Enable DIMM S3 Open: Disable DIMM S3	1-2
J7J2	Processor ThermDA and ThermDC External connection 2: Thermal DA connection 3: Ground	Open

Figure 22. Key Jumper Locations



6.5 SMBUS Headers

The SMBUS headers are used to connect the SMBUS. Refer to the following tables for pinout information.

Table 20 describes the SMBUS 3.3 V STBY pinout.

Table 20. SMBUS 3.3 V STBY Pinout

Pin	Connector Description
1	SMBDAT
2	GND
3	SMB CLK

6.6 Back Panel Connectors

The evaluation board contains a number of connectors for external system devices and peripherals. Figure 23 shows the peripheral connectors.

The following sections provide pinouts for each connector.

Figure 23. Back Panel Connectors

6.6.1 PS/2* Mouse and Keyboard Connectors

Table 21 lists the signals assigned to the PS/2* keyboard and mouse connectors. The keyboard port is on the top and the mouse port is on the bottom.

Table 21. PS/2* Mouse and Keyboard Pinout

Pin	Connector Description
1,7	Data
2,8	Reserved
3,9, 13-17	Ground
4,10	+5 V (fused)
5,11	Clock
6, 12	Reserved

6.6.2 Parallel Port

Table 22 lists the signals assigned to the parallel port connector.

Table 22. Parallel Port Connector Pinout

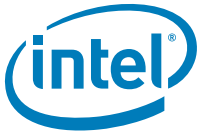
Pin	Connector Description	Pin	Connector Description
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLC IN#
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Paper end	25	Ground
13	SLCT		

6.6.3 Serial Ports

Table 23 lists the signals assigned to the serial port connector.

Table 23. Serial Port Connector Pinout

Pin	Connector Description
1	DCD
2	Serial In - RXD
3	Serial Out - TXD
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	RI



6.6.4 Dual Stacked USB Connectors

Table 24 lists the signals assigned to the dual stacked USB connector.

Table 24. USB Connector Pinout

Pin	Connector Description
1,5	Power (fused)
2,6	USBP1 # [USBP2#]
3,7	USBP1 [USBP2]
4,8	Ground

6.6.5 Video Port

Table 25 lists the signals assigned to the video port connector.

Table 25. Video Port Connector Pinout

Pin	Connector Description
1	VGA Red
2	VGA Green
3	VGA Blue
4	Monitor ID
5	GND
6	GND
7	GND
8	GND
9	GND
10	GND
11	Monitor ID
12	DDCDA
13	HSYNC
14	YSYNC
15	DDCLK

6.6.6 Dual Gigabit Ethernet Ports

Table 26 lists the signals assigned to the dual gigabit ethernet ports connector.

Table 26. Dual Gigabit Ethernet Port Connector Pinout (Sheet 1 of 2)

Pin	Connector Description
1/20	TERM
2/19	D4N
3/18	D3P
4/17	TD3
5/16	D2N
6/15	D1P

Table 26. Dual Gigabit Ethernet Port Connector Pinout (Sheet 2 of 2)

Pin	Connector Description
7/14	TD1
8/26	D4P
9/25	TD4
10/24	D3N
11/23	D2P
12/22	TD2
13/21	D1N
27/31	GRN_A
28/32	GRN_C
29/33	GRN_YEL_A
30/34	GRN_YEL_C
35/36/ 37/38	GND

7.0 Board Setup Checklist

The following is a checklist of items to ensure proper functionality of the development kit.

- All cables are properly plugged in:
  - Hard drives
  - SATA and/or IDE
  - Monitor, keyboard, mouse
  - Additional peripherals such as CD, DVD, floppy, etc.
  - Power
- Fans are securely in place and plugged into the appropriate jumpers.
- Memory, PCI, and PCI Express* cards are secured in slots.
- RTC battery is installed.
- Jumpers are configured correctly (refer to Section 6.4, "Jumpers" on page 54).
- Proper standoffs for benchtop use.

8.0 Debug Procedure

The debug procedure in this section is used to determine baseline functionality for the Intel® Core™ 2 Duo Processor and Intel® Core™ Duo Processor with Intel® E7520 Chipset Development Kit. This is a cursory set of tests designed to provide a level of confidence in the platform operation.

8.1 Level 1 Debug (Port80/BIOS)

Refer to the steps in Table 27 when debugging a board that does not boot.

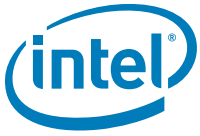
Table 27. Level 1 Debug (Port80/BIOS)

Step	Test	Passing Criteria	Cause of Failure
1	Verify "SYSTEM PWRGD" LED	Green	Power sequence failure – go immediately to Level 2 debug
2	Is "PCI Reset" LED illuminated?	Decimal on Port 80 display RED	PCI reset stuck – go to Level 3 debug
3	Verify CPURST LED is off	Off	CPU reset stuck – go to Level 3 debug
4	Verify Port 80 posting	Port 80 LEDs are posting boot codes and stopping	System Hang – Check BIOS go to level 3 debug. Refer to AMI* BIOS documentation for details.
5	Verify BIOS settings	Latest BIOS installed	Contact Intel representative for the latest BIOS image
6	Verify default jumper settings	See default settings	Improper jumper settings

8.2 Level 2 Debug (Power Sequence)

Table 28. Level 2 Debug (Power Sequence)

Step	Test	Passing Criteria	Cause of Failure
1	Primary power supply voltages	Measure voltages across: 3.3 V -12 V 5 V 5 V 12 V	External power supply failure
2	1.8V	1.8 V	DDR2 power supply failure
3	1.5V	1.5 V	MCH/ICH core power supply failure
4	1.8V VSBY	1.8 V	DDR2 standby power supply failure
5	CPU VTT Power Supply	1.05 V	CPU_VTT power supply failure
6	CPU0 VRD	1.2 V–1.4 V	CPU0 VRD failure
7	CPU1 VRD	1.2 V–1.4 V	CPU1 VRD failure
8	Verify "SYSTEM PWRGD" LED	Green	Power sequence failure



8.3 Level 3 Debug (Voltage References)

Table 29 includes the first items to look at when debugging a board that is not booting.

Table 29. Level 3 Debug (Voltage Reference)

Step	Test	Passing Criteria	Cause of Failure
1	MCH DDR2 Channel A Vref	0.9 V	Vref incorrect: check resistor values
2	MCH DDR2 Channel B Vref	0.9 V	Vref incorrect: check resistor values
3	MCH Hublink Vref	0.354 V	Vref incorrect: check resistor values
4	MCH Hublink Vswing	0.804 V	Vswing incorrect: check resistor values
5	ICH Hublink Vref	0.347 V	Vref incorrect: check resistor values
6	ICH Hublink Vswing	0.696 V	Vswing incorrect: check resistor values
7	CPU0 VTT Vref (back side of board)	0.775 V	Vref incorrect: check resistor values
8	CPU1 VTT Vref (back side of board)	0.754 V	Vref incorrect: check resistor values
9	MCH VTT Vref	0.775 V	Vref incorrect: check resistor values